



<Variant Name>



Title :

RF BD

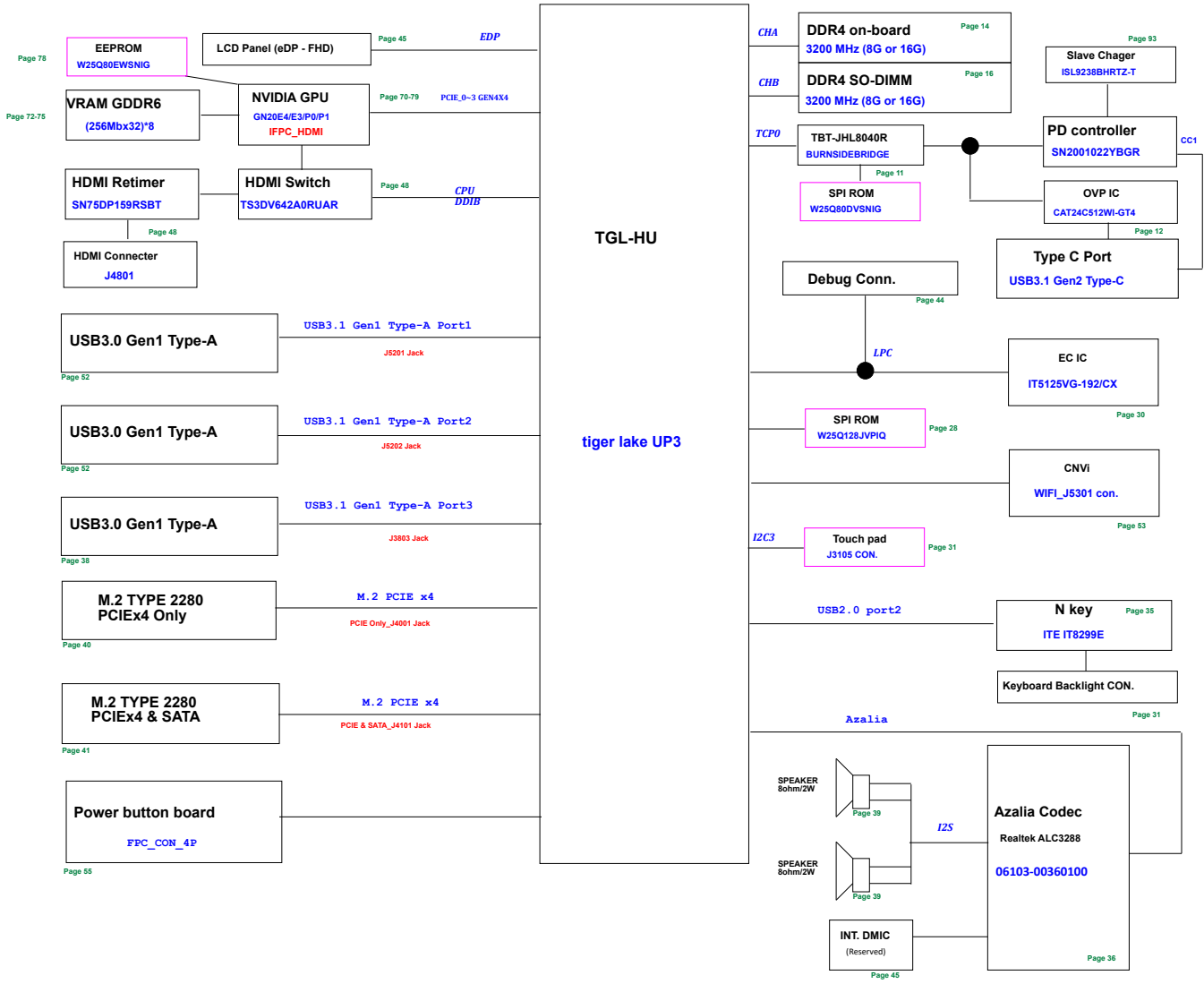
NB1-RD3EE2

Engineer: EE

Size	Project Name	Rev
A	UX482	R0.1

FX516 SCHEMATIC

BLOCK DIAGRAM



PAGE	Content
1	Block Diagram
2	System Setting
3	CPU_DMI,PEG,eDP,DDI
4	CPU_DDR
5	CPU_GND
6	CPU_CFG,RSVD
7	CPU_ESPI,SPI,SMB,CLINK
8	CPU_FCH_CSI2,EMMC,CNV
9	CPU_POWER
10	CPU_POWER_CAP
11	TBT_Titan Ridge SP
12	TBT_TFS65994ADsType C
13	TBT
14	DIM_DDR4_ON-BOARD_A(1)
15	DIM
16	DIM_DDR4 SO-DIMM B(0) TOP
17	DIM_
18	DIM_CA/DQ Voltage
19	DDR4_TERMINATION*
20	PCH_HDA,SMBUS,SYS_PWR
21	PCH-CPT(2)_PCIe,USB2,MISC
22	PCH-CPT(3)_CLK,LPC,USB3
23	PCH-CPT(4)_eDP,PCI,DP,MISC
24	PCH-CPT(5)_SPI
25	PCH-CPT(6)_GPIO
26	PCH-CPT(7)_POWER,GND
27	PCH-CPT(8)_POWER,GND
28	PCH-SPI_ROM,OTH
30	KBC_IT8995
31	EC_KB_TP
36	AUD-ALC3288
38	Audio_Jack
39	SMART AMP TAS5766M
40	Card Reader AU6465
44	BUG_Debug
45	CRT_LCD_Panel_CMOS_DMIC
48	HDMI
51	NGFF_SSD
52	USB Port
53	USB 3.0 MB Type-C
54	G-sensor
56	LED_Indicator
57	DSG_Discharge
58	PRO_PROTECT
60	DC_DC & BAT Conn.
62	ME_Conn & Skew Hole
63	EMI_RF Reserve
64	U3_B2B CONN
66	WLAN&BT SIP
67	LID_Switch / Fan_connector
70	GPU_PCIE
71	GPU_MEMORY Interface
72	Frame Buffer
74	GPU_STRAP
75	GPU_GPIO
76	GPU_VDD/GND
77	GPU_FWG Decoupling
78	GPU Power
79	VGA Sensor

- 80\_PW\_IMVP8 (1)
- 81\_PW\_IMVP8 (2)
- 83\_PW\_+1.0VSUS / +1.8VSUS
- 86\_PW\_1.2V/+0.6VS
- 87\_PW\_+3VADSW/+5VSUS
- 88\_PW\_LOAD SWITCH
- 89\_PW\_CHARGER(BQ24780)
- 90\_PW\_PROTECTION

- 91\_PW\_NVVDD
- 94\_PW\_VRAM

<Variant Name>



Project Name

**UX482**

Rev

**R0.1**

**Title :** **SKU\_Table**

Size

**Custom**

**Dept.:** **NB1-RD3EE2**

**Engineer:**

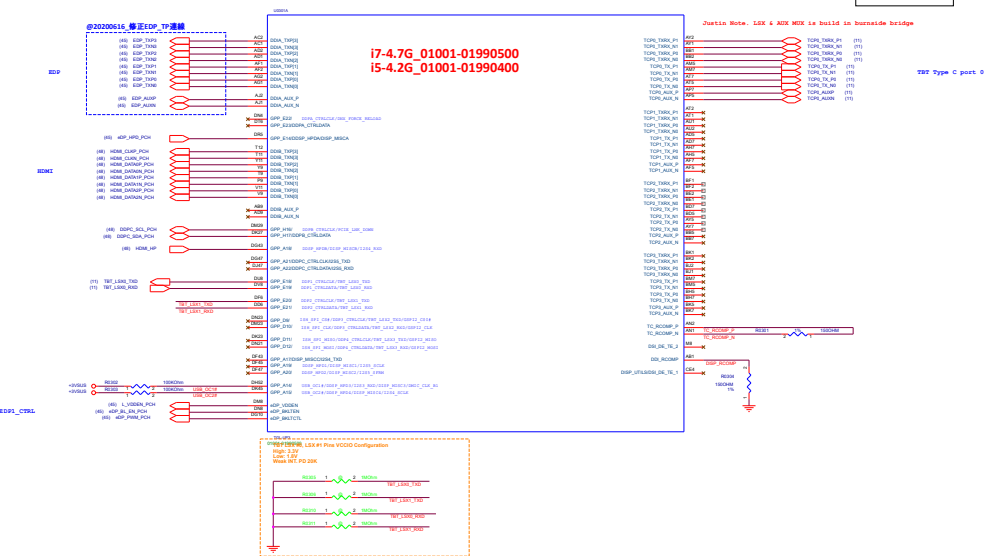
Date: **Tuesday, December 29, 2020**

Sheet

**2**

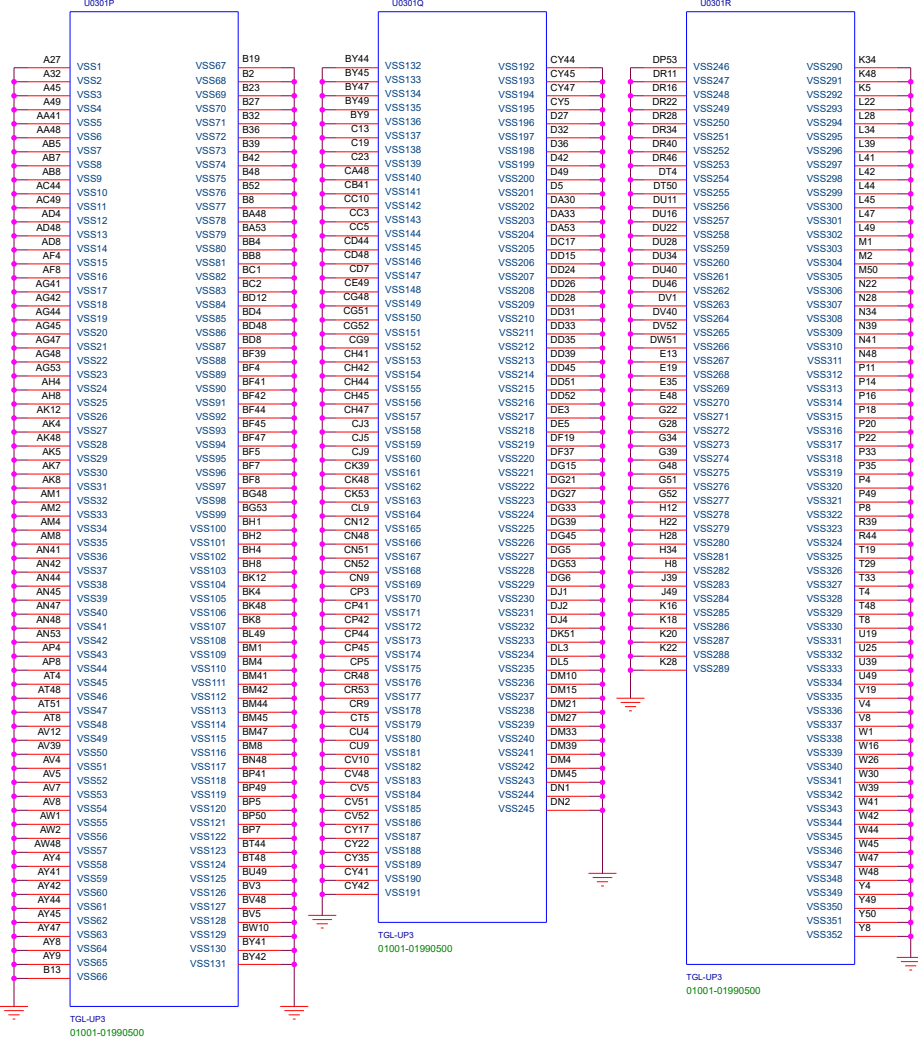
of

**102**



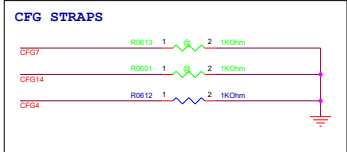
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<Variant Name>

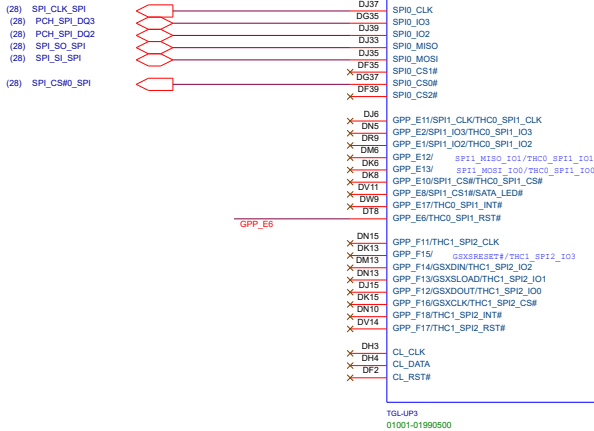
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UX482			R0.1
Title : CPU_PCH_POEWR,GND			
Size	Dept.:	Engineer:	EE
C	NB1-RD3EE2		
Date: Tuesday, December 29, 2020	Sheet	5	of 102



TDR-01P9 01001-01990500			
	1	0	NOTE
CFG4	DISABLE	ENABLE	aDP ENABLE

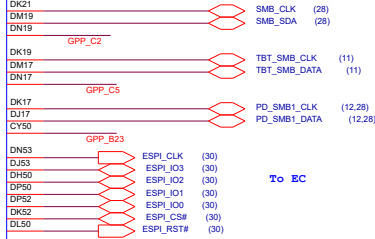
CFG	Description	Termination	Resistor
	Operation; No stall. - 0 = Stall		
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7] eDP Training: - 1 = (default) PEG Train Link - 0 = PEG Wait for BIOS for training.	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: - 1 - (Default) Normal - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[17:15]	RSVD	None	

To ROM/TPM



GPP\_B23/SM1ALERT#/PCHHOT#

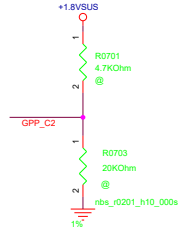
GPP\_A2/ESP1\_I02/SUBNARH#



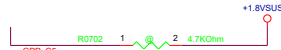
To EC

VPRO ENABLE STRAP

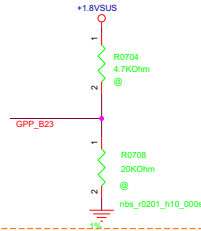
TLS CONFIDENTIALITY  
LOW: TLS CONFIDENTIALITY DISABLE  
HIGH: TLS CONFIDENTIALITY ENABLE  
WEAK INT.PD 20K  
Must be pulled up to support  
Intel AMT with TLS.



BFX STRAP 1 -BIT1 WEAK INT.PD 20K



CFUNSSC CLOCK FREQ  
HIGH:19.2MHZ CLOCK FROM DIVIDER  
(DERIVED FROM 38.4MHZ CRYSTAL)  
LOW: 38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT)  
WEAK INT.PD 20K

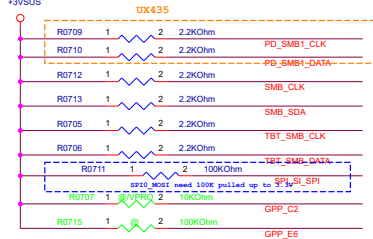


To SO-DIMM

Reserved for TBT Vpro

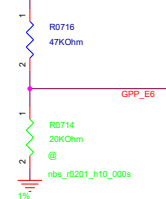
to PD

+3VSUS



+1.8VSUS

Follow Intel TGL-UP3 CRB



<Variant Name>

Project Name		Rev
ASUS UX482		R0.1
Title : CPU_LPC,SPI,SMB,CLINK		

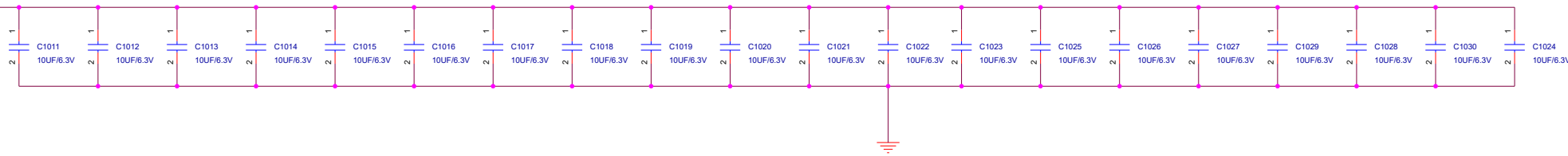
Size	Dept.:	Engineer:
C	NB1-RD3EE2	EE
Date: Tuesday, December 29, 2020	Sheet	7 of 102





+VCCIN

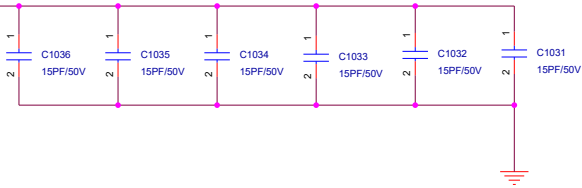
TGL UP3 ICmax=65A (0402 10uF \*12)



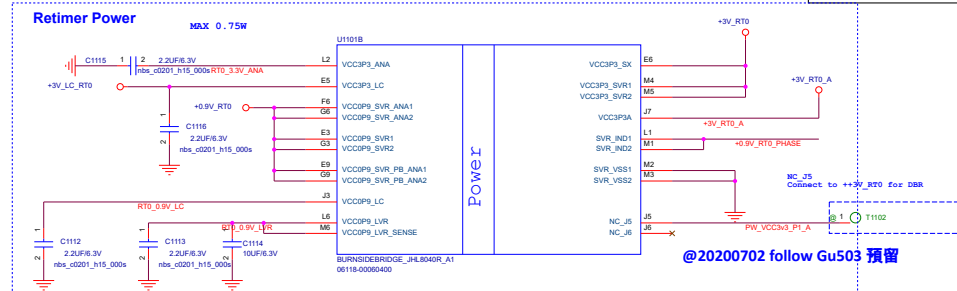
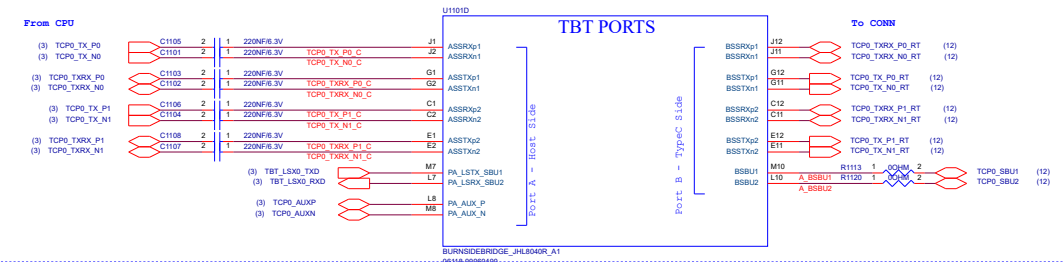
@20200616\_add C1031~36: 15PF for EMI/RF

+VCCIN

TGL IVR decoupling Caps

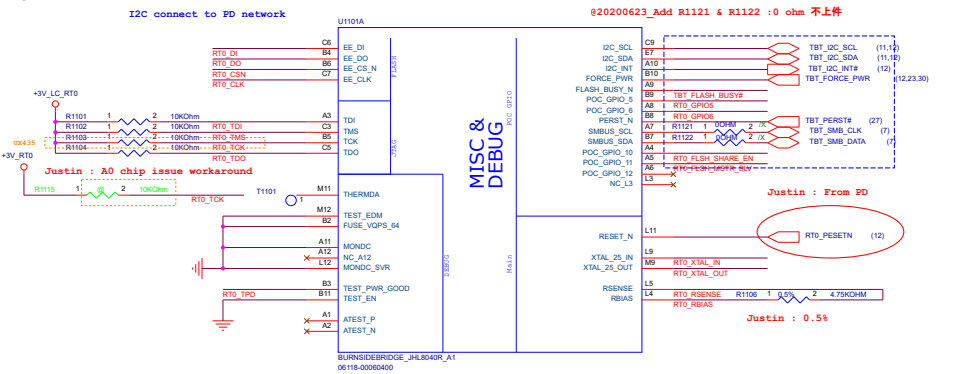


## 20GBPS TBT LINK PORT 0



**MISC** Justin: SMBUS for Vpro

Justin: SMBUS for Vpro

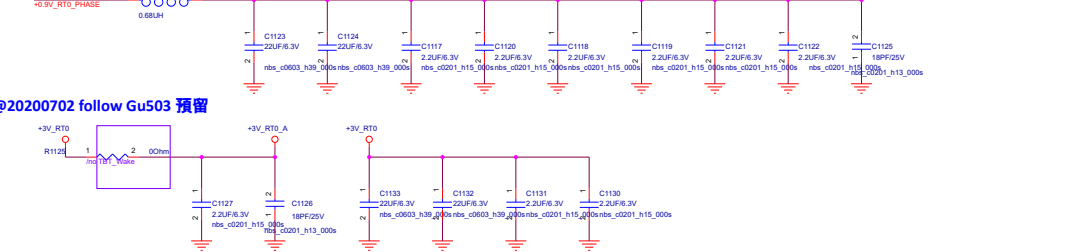


## Decoupling

[Inductor colay footprint] R1.0E

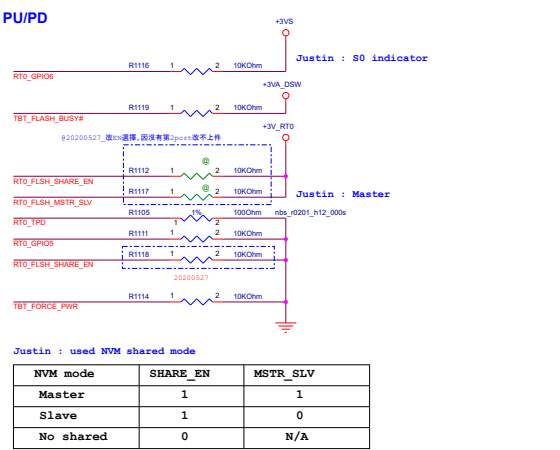
1st source : 09016-00122200  
2nd source : 09016-00121400

2



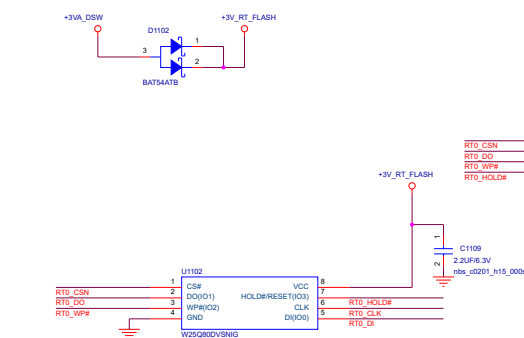
@20200702 follow Gu503 預留

@20200611\_C1110 & C1111 將18PF改22PCF

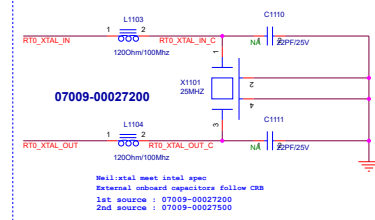


NVM mode	SHARE_EN	MSTR_SLV
Master	1	1
Slave	1	0
No shared	0	N/A

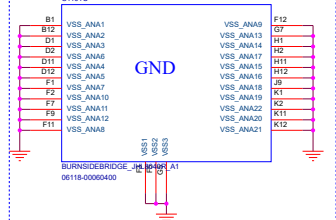
## Flash ROM



25Mhz Xtal

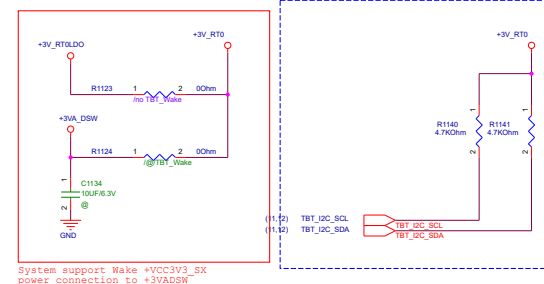


## GND



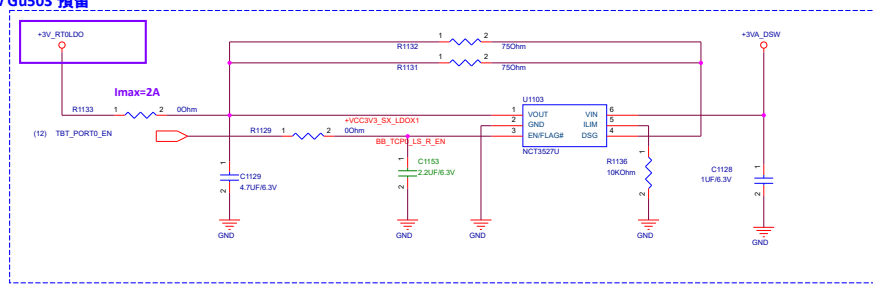
```
@2020831_TBT_I2C_SCL/TBT_I2C_SDA PU +3V_RT0
```

@20200702 follow Gu503 預留

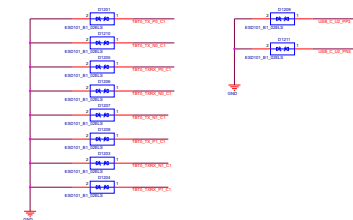
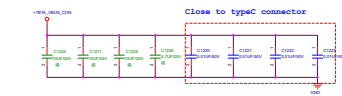
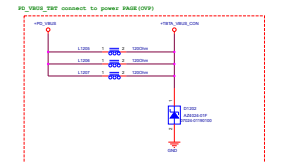
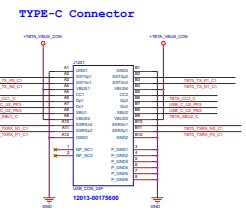
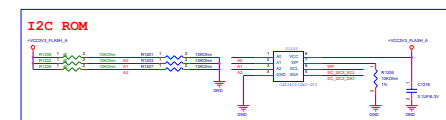
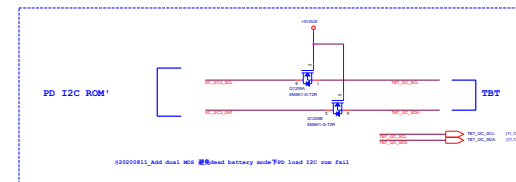
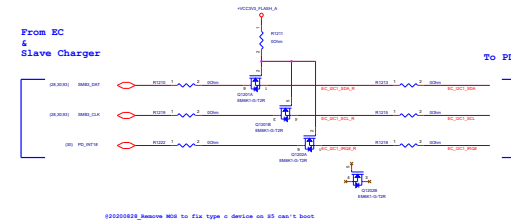
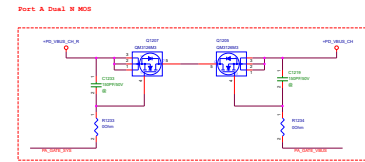
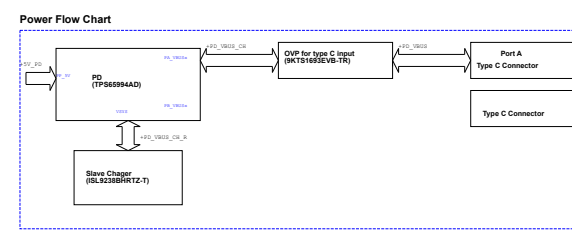
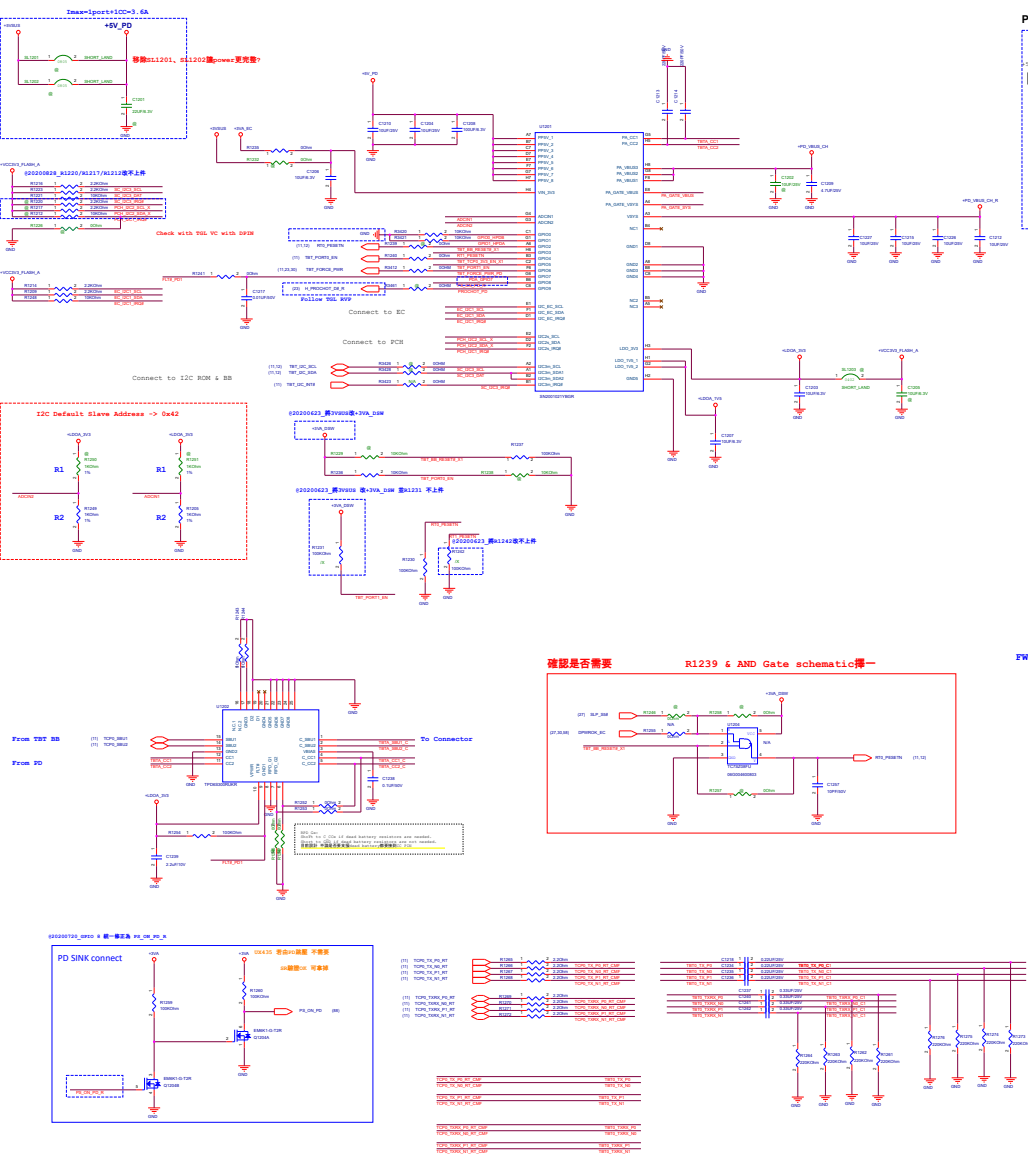


System support Wake +VCC3V3\_SX  
power connection to +3VADSW

@20200702 follow Gu503 預留




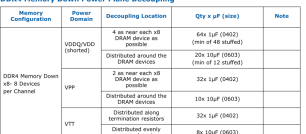
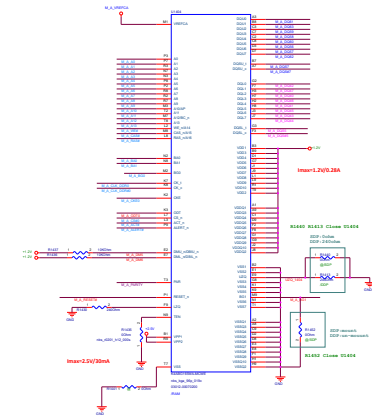
**Check which power solution should be used**




teknisi indonesia



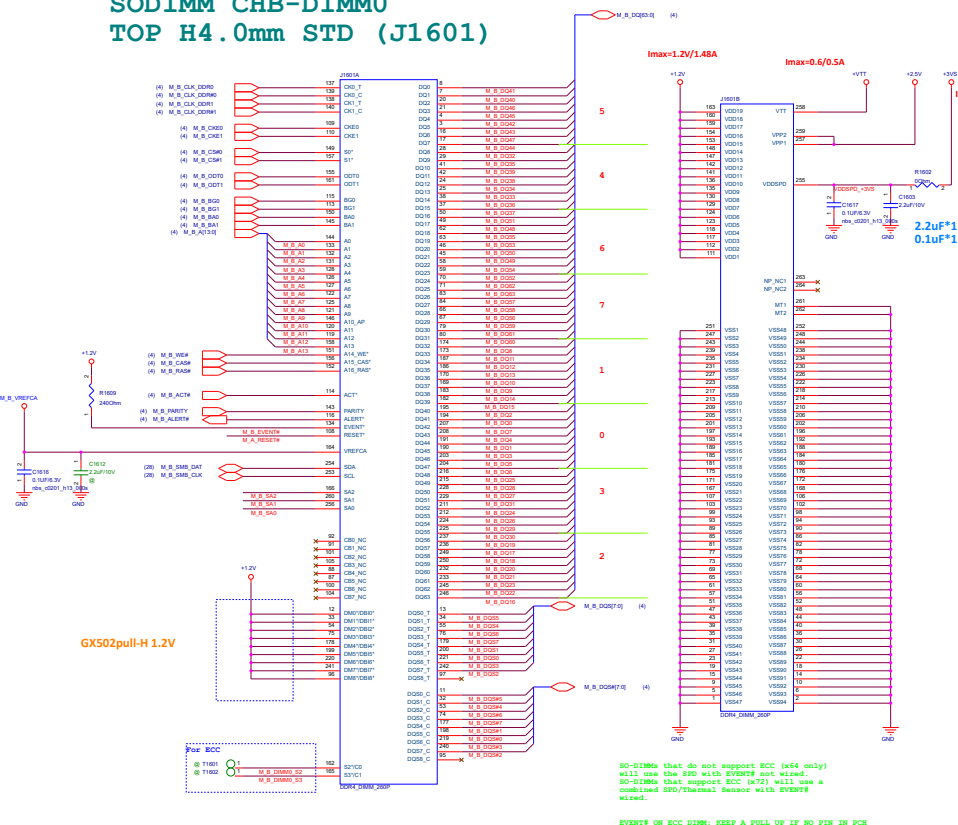
		<b>Title :</b> <b>DDR4_TERMINATION</b>	
<b>ASUSTeK COMPUTER INC.</b>		<b>Engineer:</b> <b>EE</b>	
Size <b>A</b>	Project Name <b>GX502GX</b>		Rev <b>R1.2</b>
Date: <b>Tuesday, December 29, 2020</b>		Sheet <b>13</b> of <b>102</b>	



<Variant Name>

		Title : <b>DDR4_ON-BOARD_A2</b>	
NB1-RD3EE2		Engineer: <b>EE</b>	
Size <b>Custom</b>	Project Name <b>UX482</b>		Rev <b>R0.1</b>
Date: <b>Tuesday, December 29, 2020</b>		Sheet <b>15</b> of <b>102</b>	

SODIMM CHB-DIMM0  
TOP H4.0mm STD (J1601)

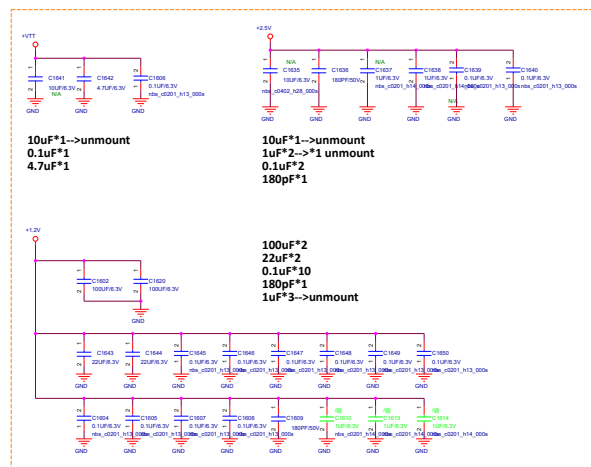
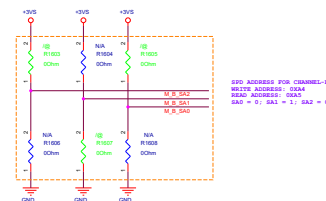


#### Table 4-24. DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x $\mu$ F (size)
DDR4 2 Channels SODIMM <b>1DPC</b>	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10 $\mu$ F (0603)
		4 near each side of the DIMM connector close to VDD pins	16x 1 $\mu$ F (0402)
		1 placeholder	1x 330 $\mu$ F (7343)
	VTT	Placed on VTT plane close to DIMM, 1 cap stuffed, 1 placeholder	2x 10 $\mu$ F (0603)
		Placed on VTT plane close to DIMM	4x 1 $\mu$ F (0402)
	VPP	DIMM Pin side, 1 per DIMM	2x 10 $\mu$ F (0603)
		DIMM Pin side, 1 per DIMM	2x 1 $\mu$ F (0402)
	VDDSPD	Place close to DIMM	2x 0.1 $\mu$ F (0402)
		Place close to DIMM	2x 2.2 $\mu$ F (0402)




@20200619\_依照公版修改SA2=0/ SA1=1/ SA0=0

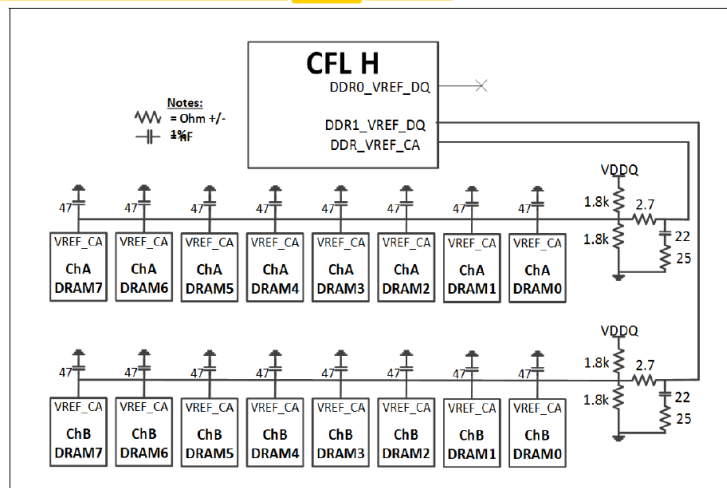


Follow FP6 CRB CAP number  
@20190701A

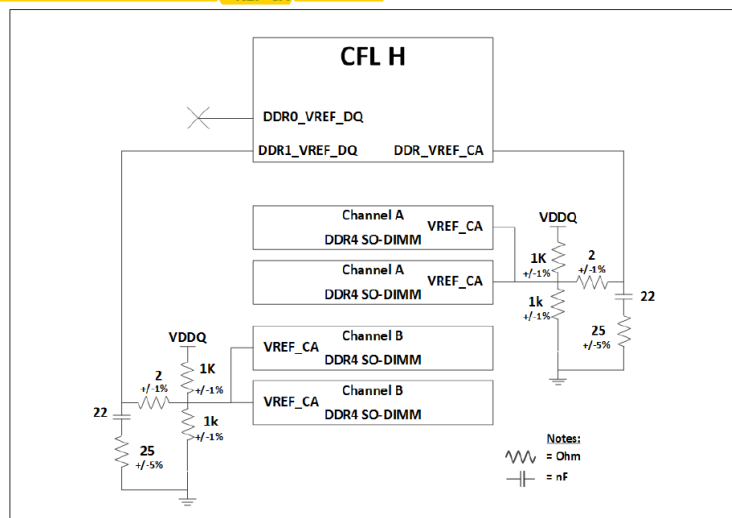
<Variant Name>

		Title : <b>DDR4_ON-BOARD_A2</b>	
NB1-RD3EE2		Engineer: <b>EE</b>	
Size <b>Custom</b>	Project Name <b>UX482</b>		Rev <b>R0.1</b>
Date: <b>Tuesday, December 29, 2020</b>		Sheet <b>17</b> of <b>102</b>	

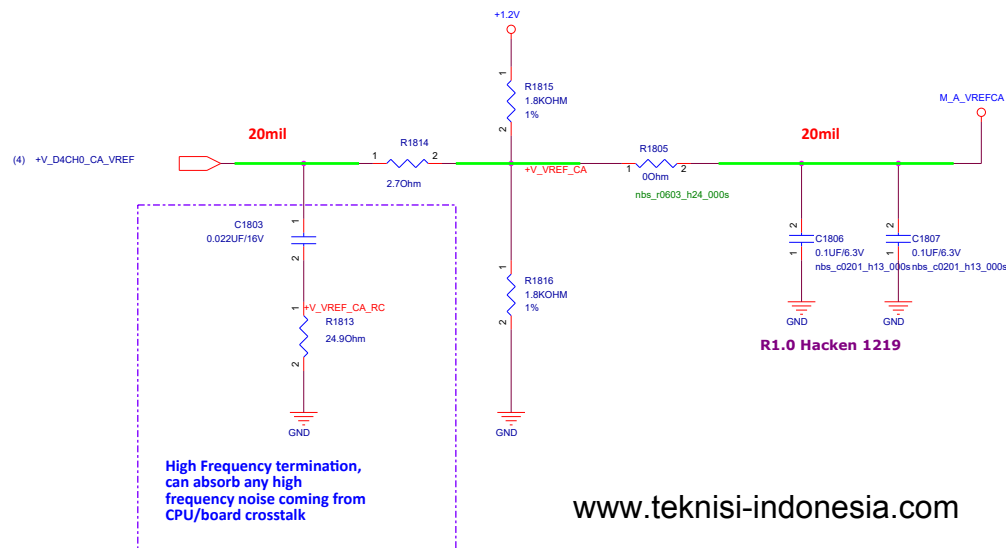
**Figure 4-24. CFL-H DDR4 x8 Memory Down  $V_{REF-CA}$  Overview**



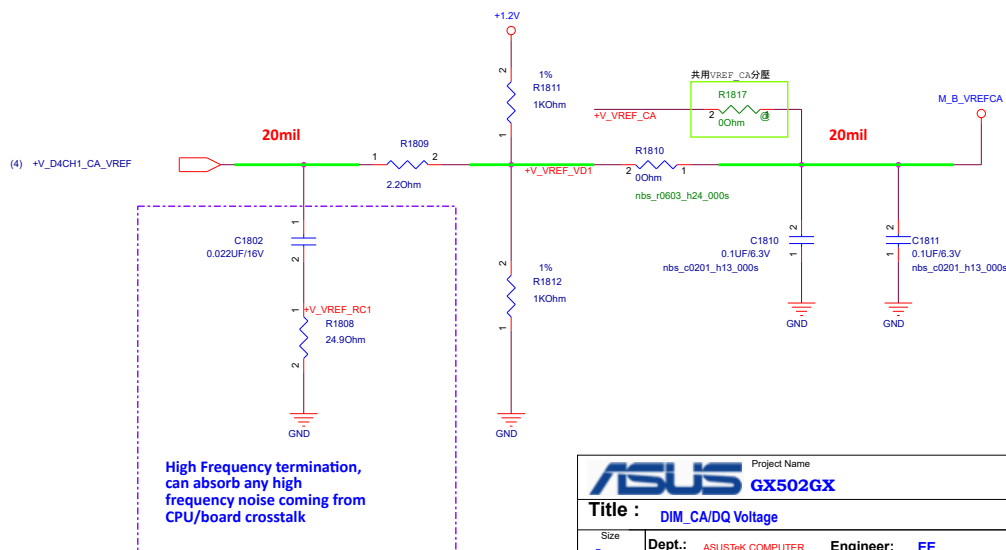
**Figure 4-22. CFL-H DDR4 SO-DIMM V<sub>REF-CA</sub> Overview**

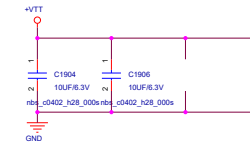
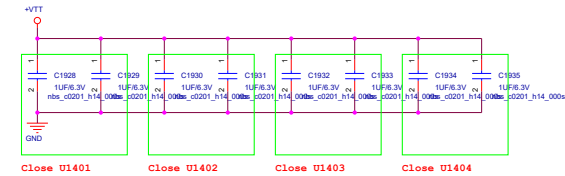


## Memory Down Vref

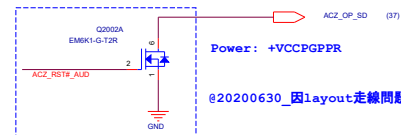
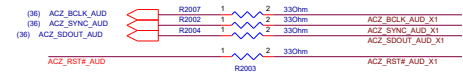


## SO-DIMM1 Vref

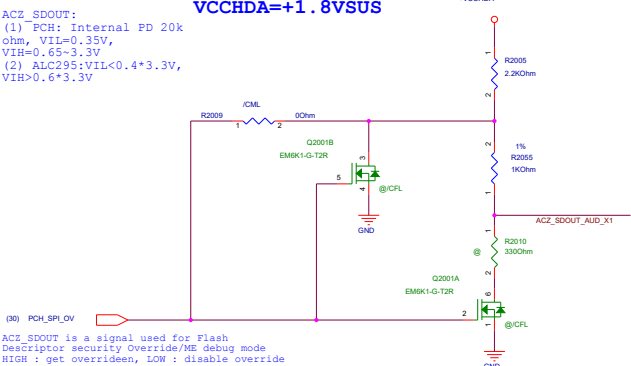




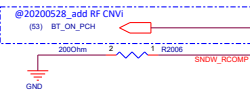
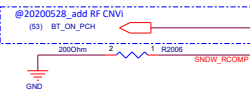
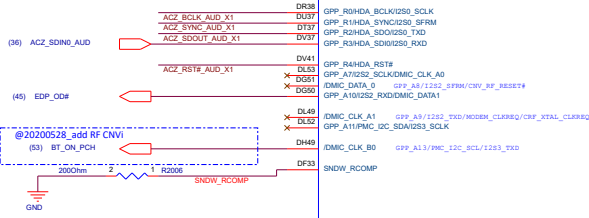
HD Audio



@20200817\_Follow Gaming畫法



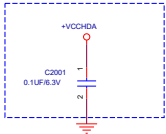
VCCHDA=+1.8VSUS



01001-01990000

TGL-UP3

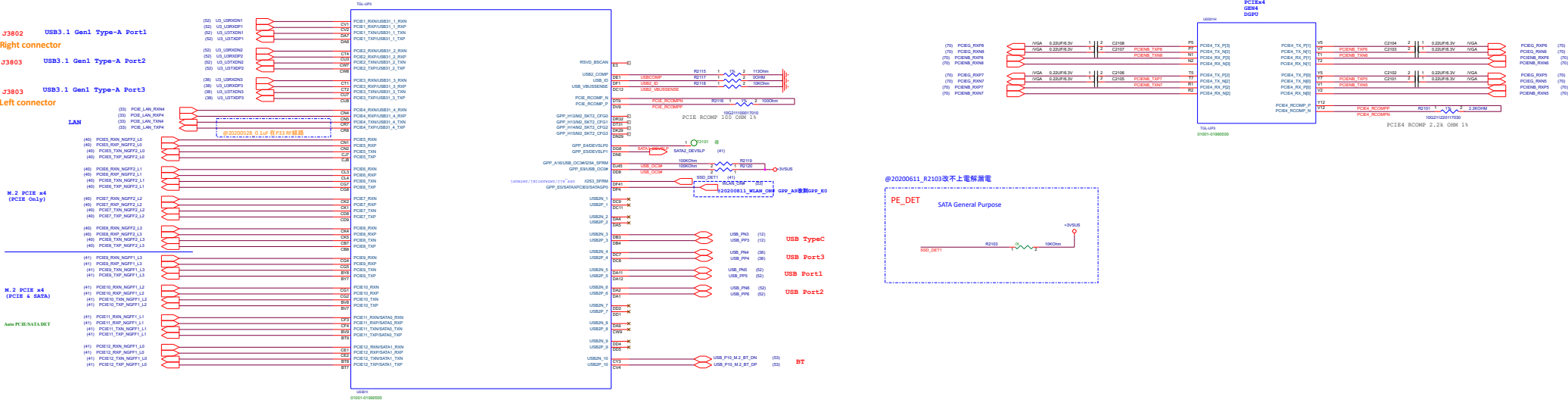
@20200612\_add C2001 for CRB  
close to the PCH ball



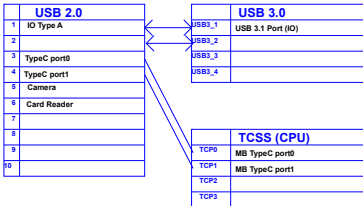
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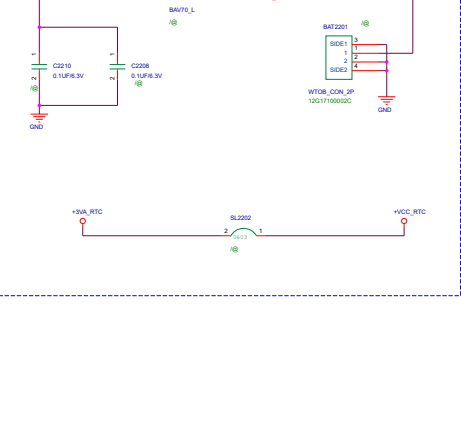
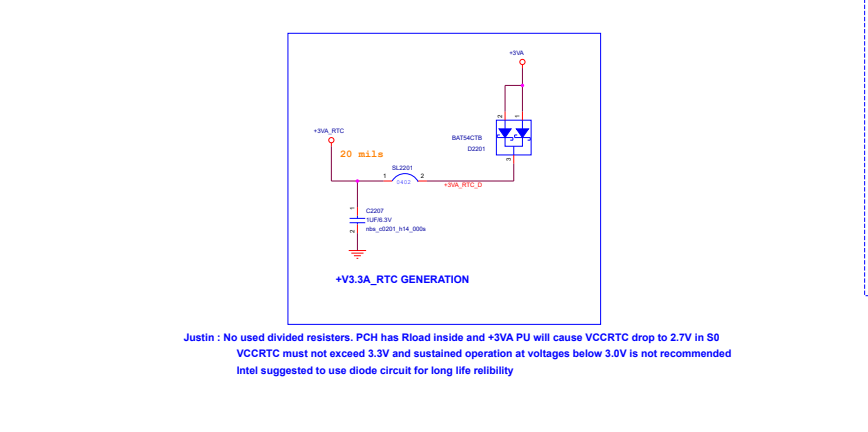
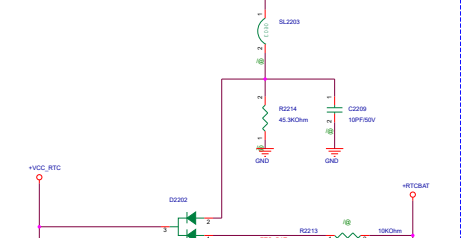
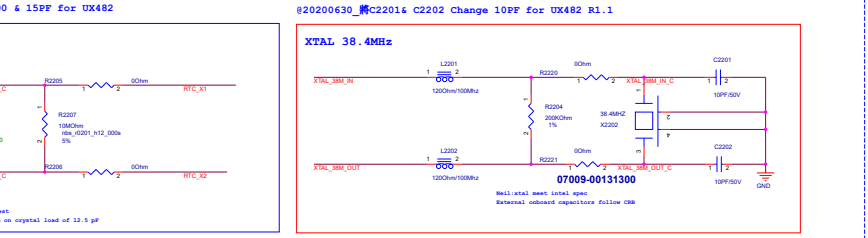
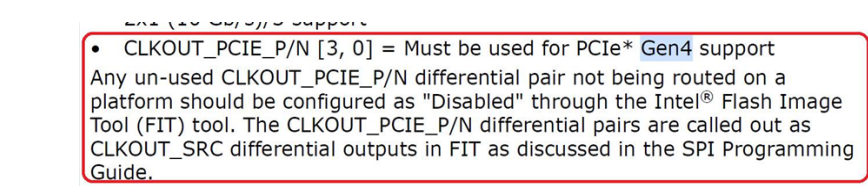
ASUS		Project Name	Rev
UX482			RD.1
Title : CPU_PCH_AUDIO.S010.S0XC			
Size	Dept.: NB1-RD3EE2	Engineer: EE	
D	Date: Tuesday, December 29, 2020	Sheet	20 of 102

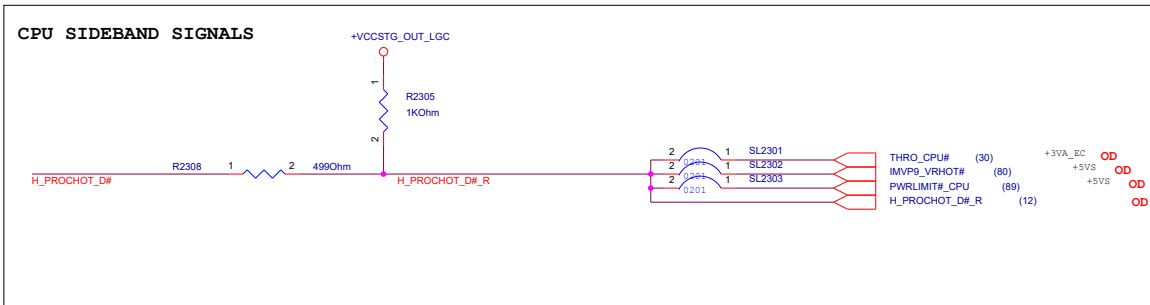
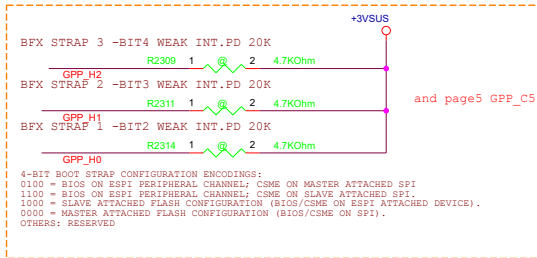
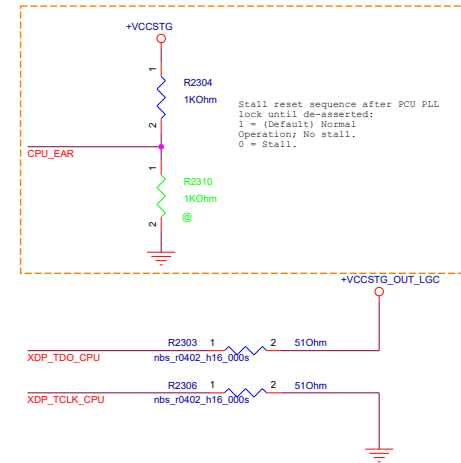
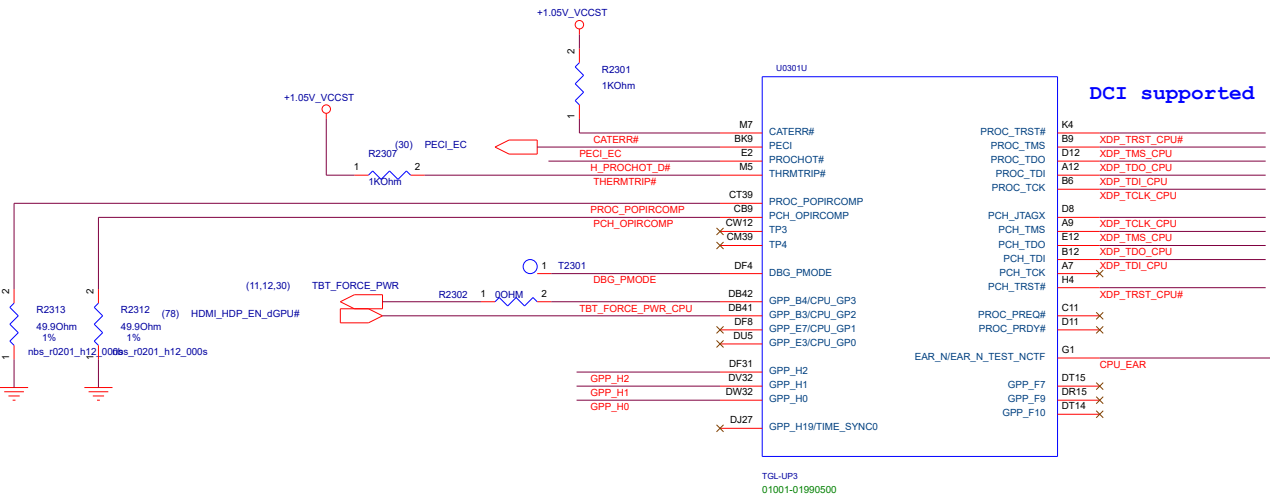





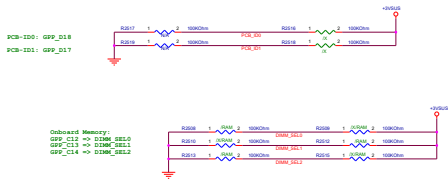
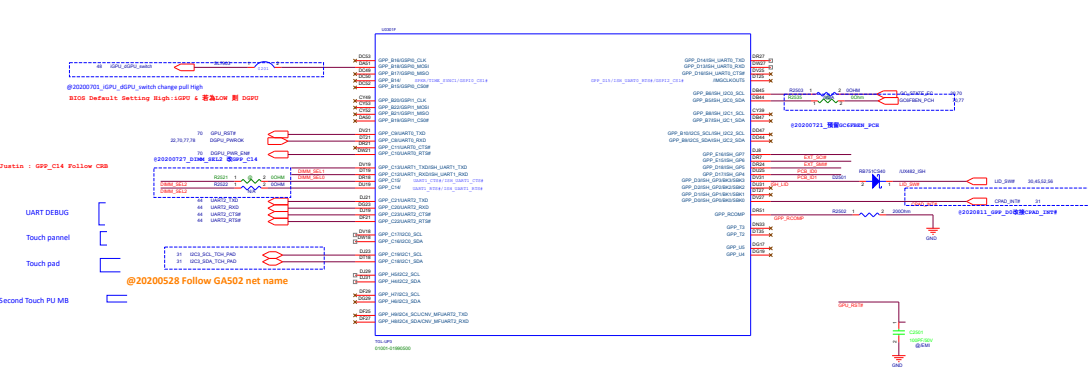
PCI-B* X1	PCIe USAGE SERIALS/OPTION	Co-1ay	Clock
PCI-B_1	N/A		
PCI-B_2	N/A		
PCI-B_3	N/A		
PCI-B_4	N/A		
PCI-B_5	N/A		
PCI-B_6	N/A		
PCI-B_7	N/A		
PCI-B_8	N/A		
PCI-B_9	N/A		
PCI-B_10	N/A		
PCI-B_11	N/A		
PCI-B_12	N/A		
PCI-B_13	N/A		
PCI-B_14	N/A		
PCI-B_15	N/A		
PCI-B_16	N/A		
PCI-B_17	N/A		
PCI-B_18	N/A		
PCI-B_19	N/A		
PCI-B_20	N/A		
PCI-B_21	N/A		
PCI-B_22	N/A		
PCI-B_23	N/A		
PCI-B_24	N/A		
PCI-B_25	N/A		
PCI-B_26	N/A		
PCI-B_27	N/A		
PCI-B_28	N/A		
PCI-B_29	N/A		
PCI-B_30	N/A		
PCI-B_31	N/A		
PCI-B_32	N/A		
PCI-B_33	N/A		
PCI-B_34	N/A		
PCI-B_35	N/A		
PCI-B_36	N/A		
PCI-B_37	N/A		
PCI-B_38	N/A		
PCI-B_39	N/A		
PCI-B_40	N/A		
PCI-B_41	N/A		
PCI-B_42	N/A		
PCI-B_43	N/A		
PCI-B_44	N/A		
PCI-B_45	N/A		
PCI-B_46	N/A		
PCI-B_47	N/A		
PCI-B_48	N/A		
PCI-B_49	N/A		
PCI-B_50	N/A		
PCI-B_51	N/A		
PCI-B_52	N/A		
PCI-B_53	N/A		
PCI-B_54	N/A		
PCI-B_55	N/A		
PCI-B_56	N/A		
PCI-B_57	N/A		
PCI-B_58	N/A		
PCI-B_59	N/A		
PCI-B_60	N/A		
PCI-B_61	N/A		
PCI-B_62	N/A		
PCI-B_63	N/A		
PCI-B_64	N/A		
PCI-B_65	N/A		
PCI-B_66	N/A		
PCI-B_67	N/A		
PCI-B_68	N/A		
PCI-B_69	N/A		
PCI-B_70	N/A		
PCI-B_71	N/A		
PCI-B_72	N/A		
PCI-B_73	N/A		
PCI-B_74	N/A		
PCI-B_75	N/A		
PCI-B_76	N/A		
PCI-B_77	N/A		
PCI-B_78	N/A		
PCI-B_79	N/A		
PCI-B_80	N/A		
PCI-B_81	N/A		
PCI-B_82	N/A		
PCI-B_83	N/A		
PCI-B_84	N/A		
PCI-B_85	N/A		
PCI-B_86	N/A		
PCI-B_87	N/A		
PCI-B_88	N/A		
PCI-B_89	N/A		
PCI-B_90	N/A		
PCI-B_91	N/A		
PCI-B_92	N/A		
PCI-B_93	N/A		
PCI-B_94	N/A		
PCI-B_95	N/A		
PCI-B_96	N/A		
PCI-B_97	N/A		
PCI-B_98	N/A		
PCI-B_99	N/A		
PCI-B_100	N/A		



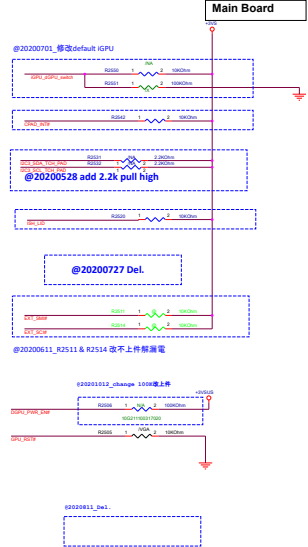


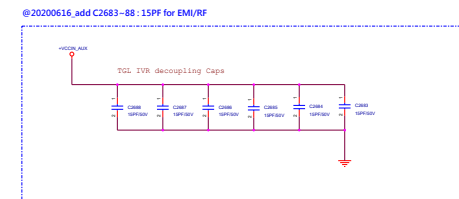
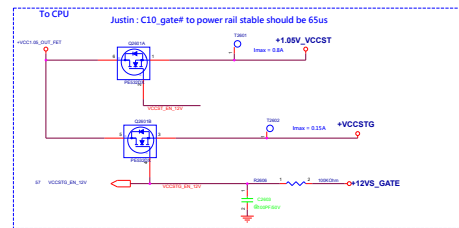
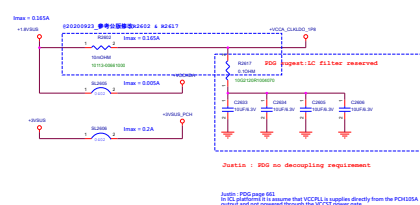
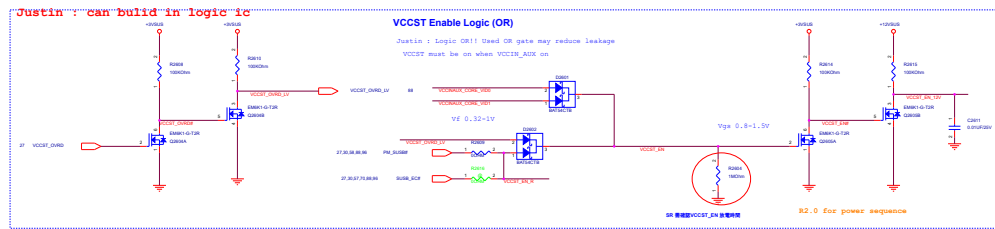
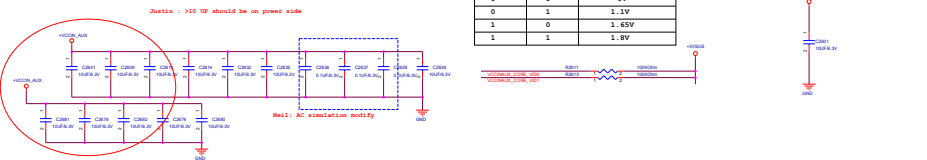
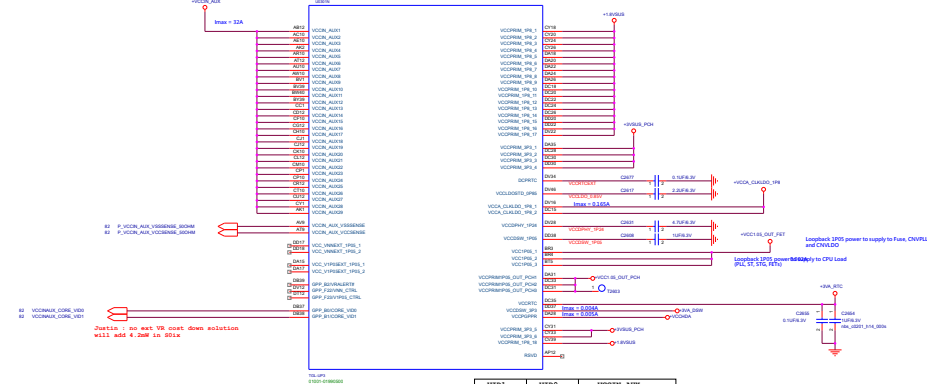


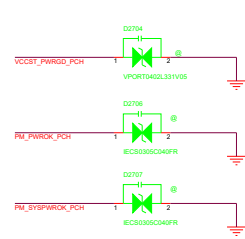
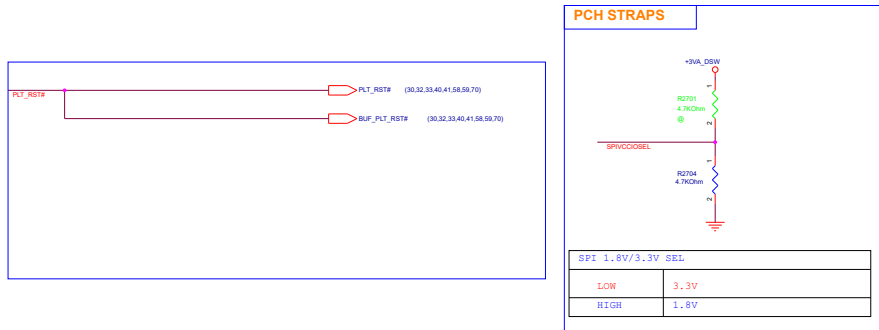
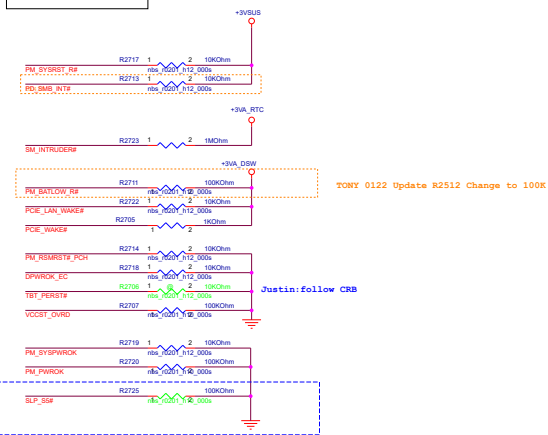
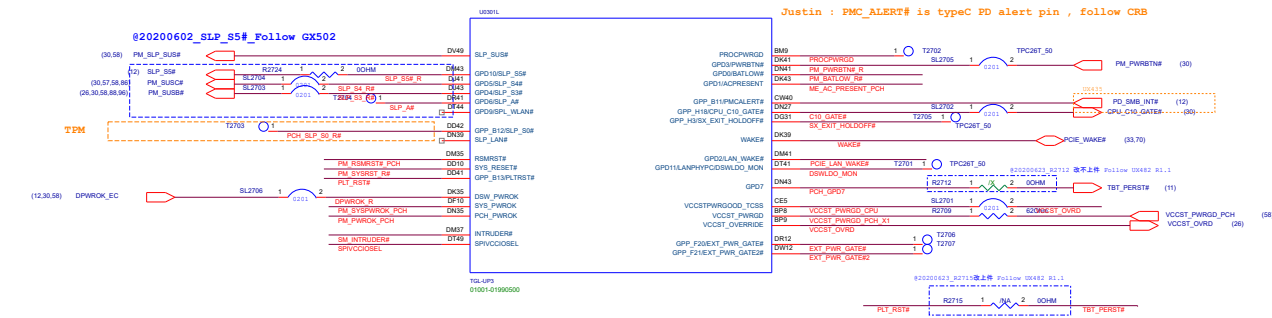
		Project Name		Rev
		UX482		R0.1
Title : PCH-SPI ROM,OTH				
Size	Dept.:		Engineer:	
C	NB1-RD3EE2		EE	
Date: Tuesday, December 29, 2020			Sheet	24 of 102



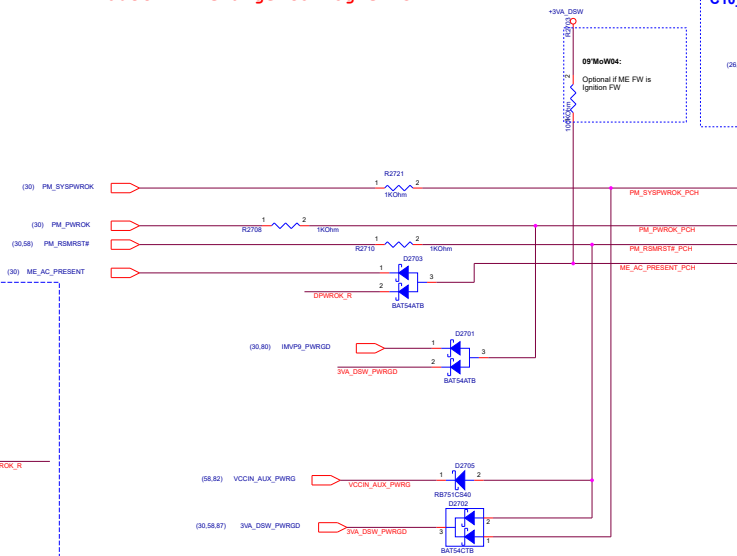
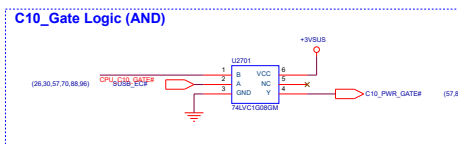
MEMORY DOWN Table			D18M_SEL4			Key Part List		
			PCB_ID1	PCB_ID2	PCB_ID3			
			2	1	0			
03012-00070200	SKJ23 目前線路	Samung 1GB	0	0	0	上替: R2509 / R2512 / R2513 下上替: R2509 / R2512 / R2513		
			0	0	1			
03012-00040600	SKJ4	MICRO 8Gb	0	1	0	上替: R2508 / R2512 / R2513 下上替: R2509 / R2512 / R2513		
03012-00040700	SKJ2	Samung 8Gb	0	1	1	上替: R2509 / R2512 / R2513 下上替: R2509 / R2512 / R2513		
			1	0	0			
03012-00070300	SKJ1	Bynix 16Gb	1	0	1	上替: R2509 / R2510 / R2515 下上替: R2509 / R2512 / R2513		
			1	1	1			







Justin : change to logic IC



Power failure solution (S0-->G3,S5-->G3):

Justin : take DSW\_PWROK low on emergency power loss, it must also take RSMRST# low at the same time

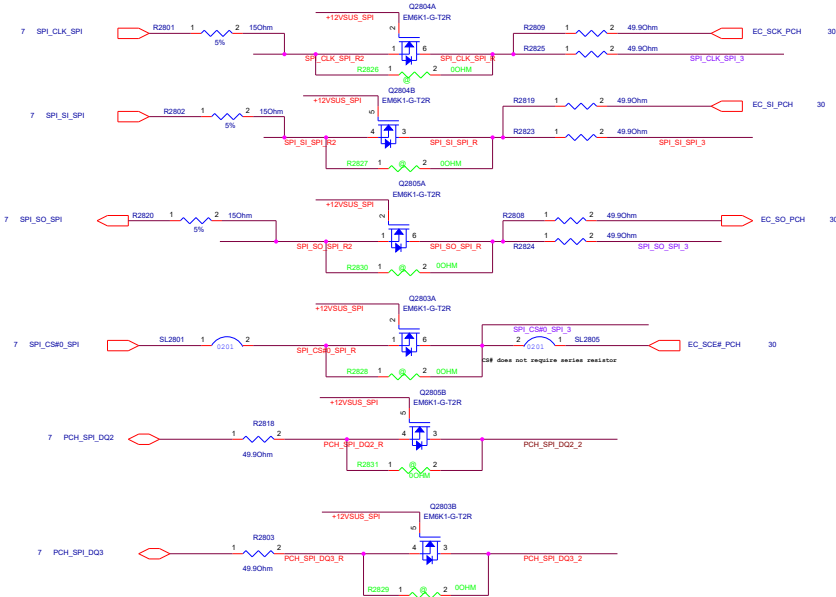
## System Management Interface

Note. No TPM : R1 22 ohm  
R2 75 ohm  
R3 22 ohm  
R4 X

The diagram shows a circuit for SPI interface. It includes two resistors, R2815 and R2810, both rated at 100K Ohm. R2815 is connected between a +12V supply and a node. R2810 is connected between a +5V supply and the same node. The node is connected to a 20mil trace labeled +12V3V3\_SPI.

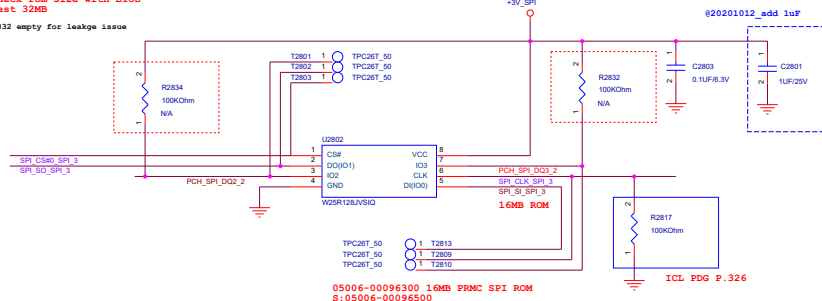
@20200611 新增R2810 Pull 5VSUS  
並將R2815改不上件,解漏電

## EC,SPI ROM Side

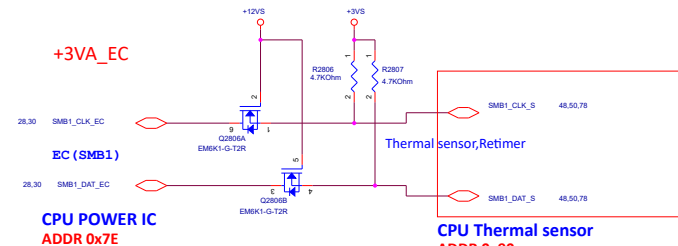


Justin : check rom size with BIOS  
Intel suggest 32MB

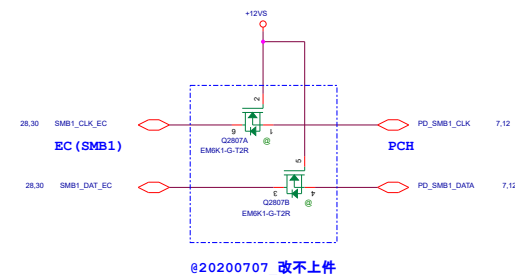
6/6 R2834,R2832 empty for leakge issue



05006-00096300 16MB PRMC SPI ROM  
S:05006-00096500



- CPU Thermal sensor  
ADDR 0x90
- VRAM Thermal sensor  
ADDR 0x91
- GPU Thermal sensor  
ADDR 0x92




@20200707\_改不上件


@20200602 Remove SMB\_CLK to AMP & NVVDD CLK Switch

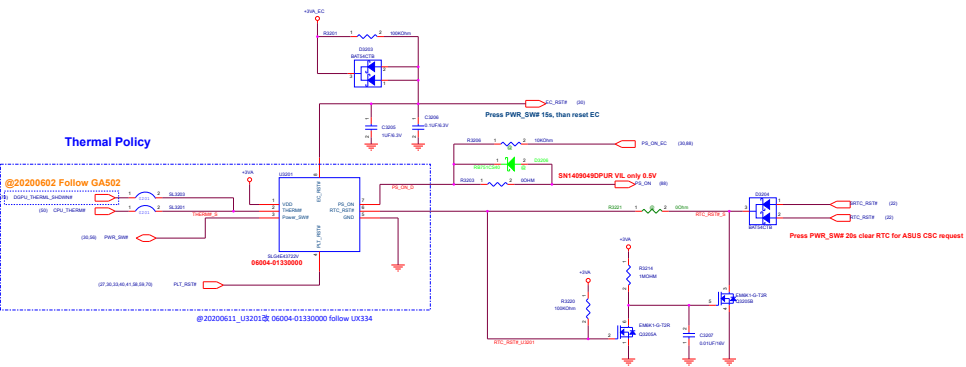
[illegible]

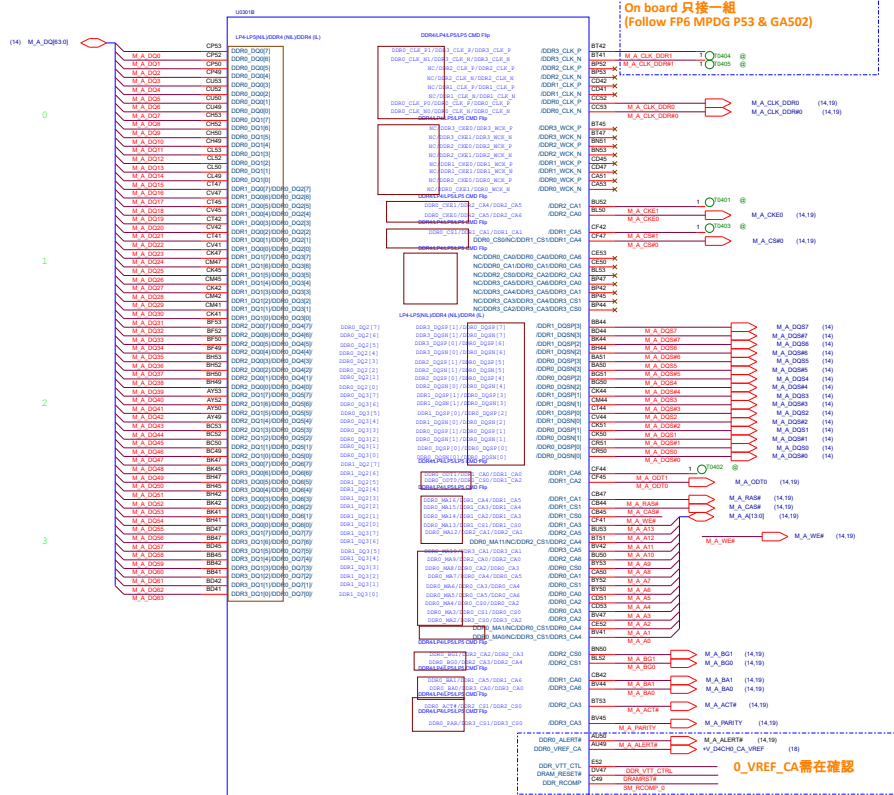
<Variant Name>

		Project Name <b>FX516PR</b>	Rev <b>R0.1</b>
<b>Title :</b> <b>PCH-SPI ROM,OTH</b>			
Size <b>C</b>	<b>Dept.:</b> <b>NBI-RD3SE2</b>		<b>Engineer:</b> <b>EE</b>
Date: <b>Tuesday December 29, 2020</b>		Sheet <b>98</b>	of <b>102</b>



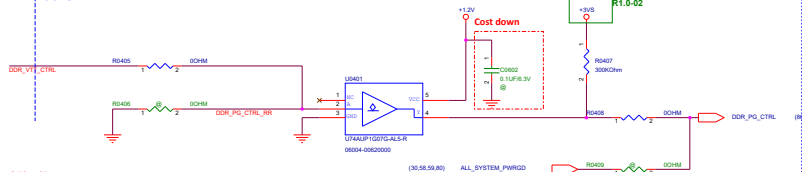
		Project Name		Rev
		<b>UX482</b>		R0.1
<b>Title :</b> <b>Test Point</b>				
Size	<b>Dept.:</b> <b>NB1-RD3EE2</b>		<b>Engineer:</b>	<b>EE</b>
B				
Date: <b>Tuesday, December 29, 2020</b>			Sheet	<b>29</b> of <b>102</b>



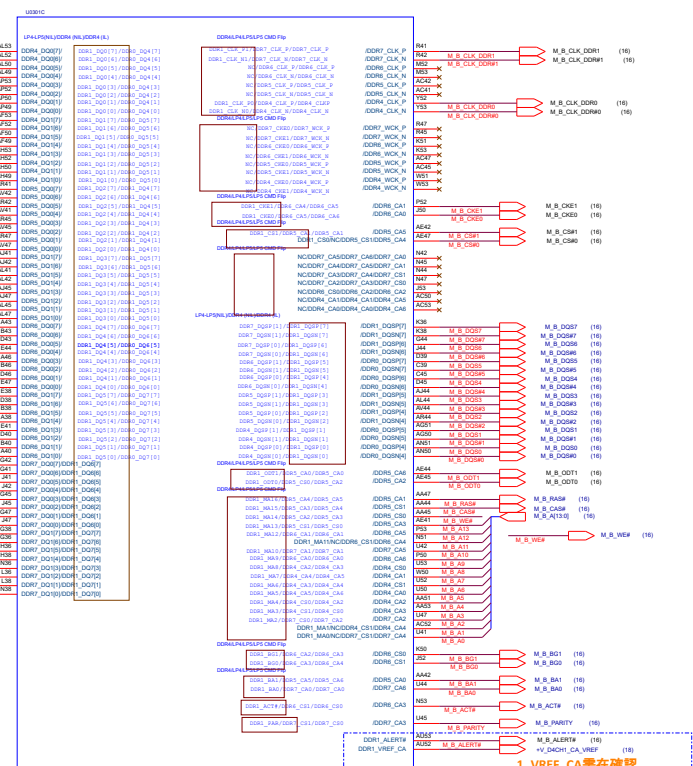


```
DDR_VTT_CTRL:
System Memory Power Gate Control:
Disables the platform memory VTT regulator
in C8 and deeper and S3.
Ref: Intel 570805 Coffeelake EDS Vol 1 Rev1.5 P.116
```

VTT Enable



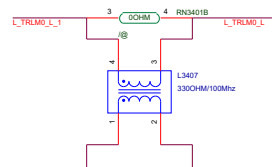
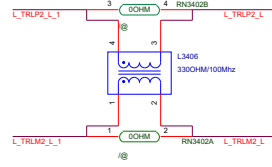
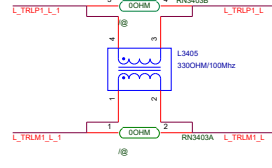
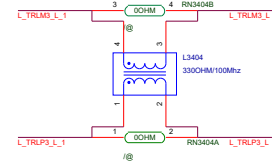
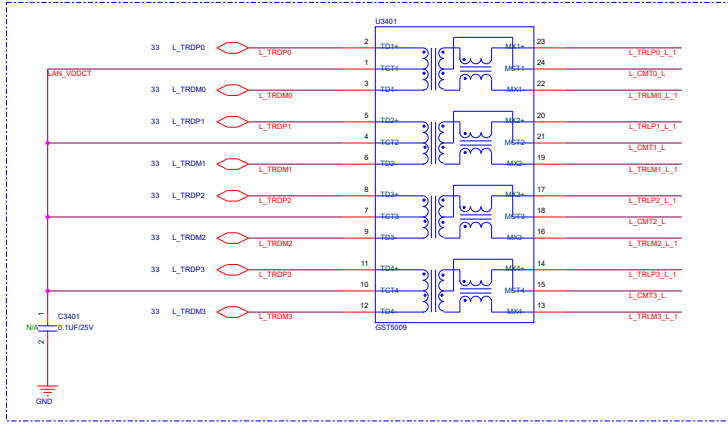
**[ 建議用料 ]**  
1st. : LOGIC U74AUP1G07G-AL5-R 06004-00620000  
2nd. : LOGIC 74AUP1G07SE-7 SOT353 06004-00051800



1 VREF CA需在確認

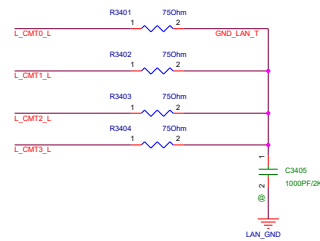
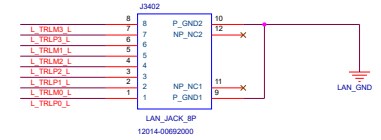


@20200702\_Rf要求修改連線順序

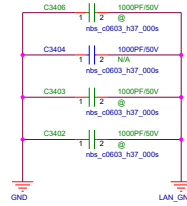


Main Board

LAN Connector



EMI



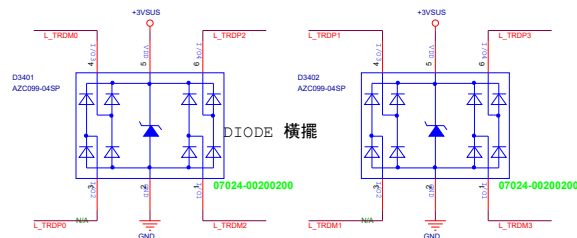
Place near chassis GND

D3401,D3402 ESD Diode

1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

GND\_LAN\_T 上禁止加任何零件

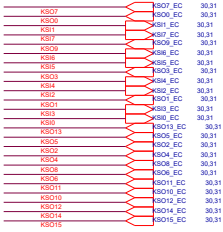
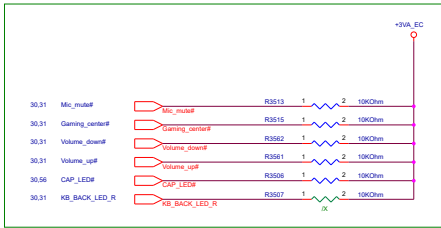
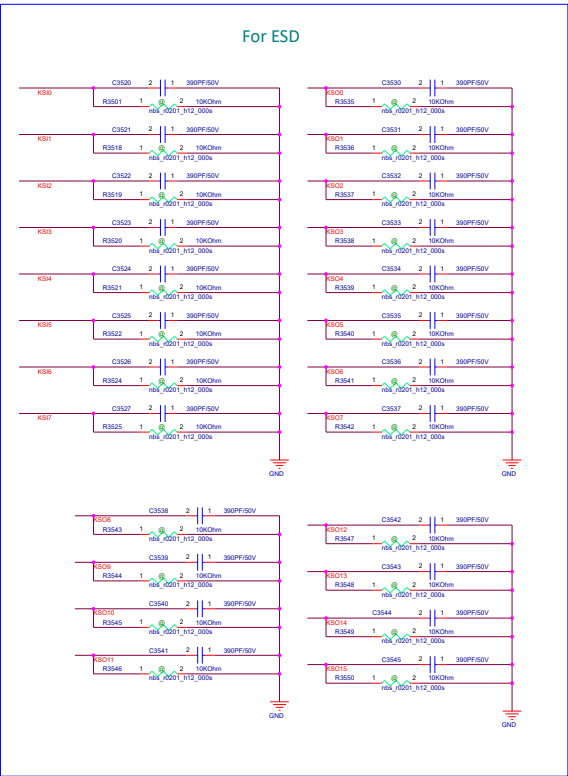


D3401,D3402 ESD Diode

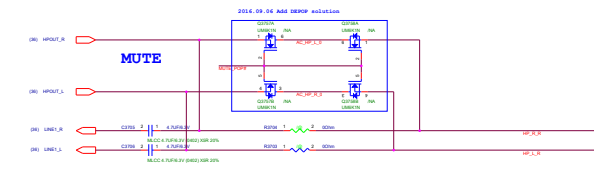
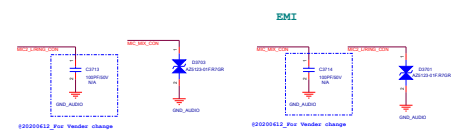
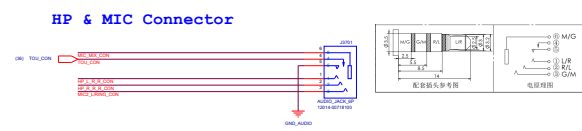
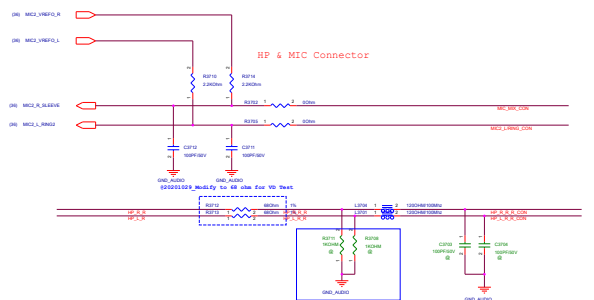
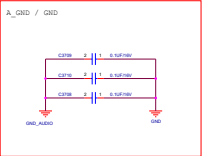
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

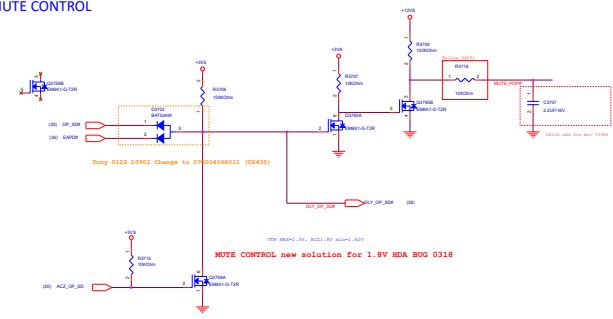
Pull up





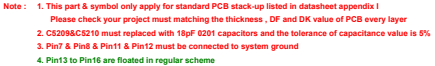


MUTE CONTROL





### USB3.1 Direct





2 nd NGFF PCIE x4 (PCIE only)

PCIE8  
NGFF2 PCIE Lane3

- (21) PCIE8\_RXN\_NGFF2\_L3
- (21) PCIE8\_RXP\_NGFF2\_L3
- (21) PCIE8\_TXN\_NGFF2\_L3
- (21) PCIE8\_TXP\_NGFF2\_L3

PCIE7  
NGFF2 PCIE Lane2

- (21) PCIE7\_RXN\_NGFF2\_L2
- (21) PCIE7\_RXP\_NGFF2\_L2
- (21) PCIE7\_TXN\_NGFF2\_L2
- (21) PCIE7\_TXP\_NGFF2\_L2

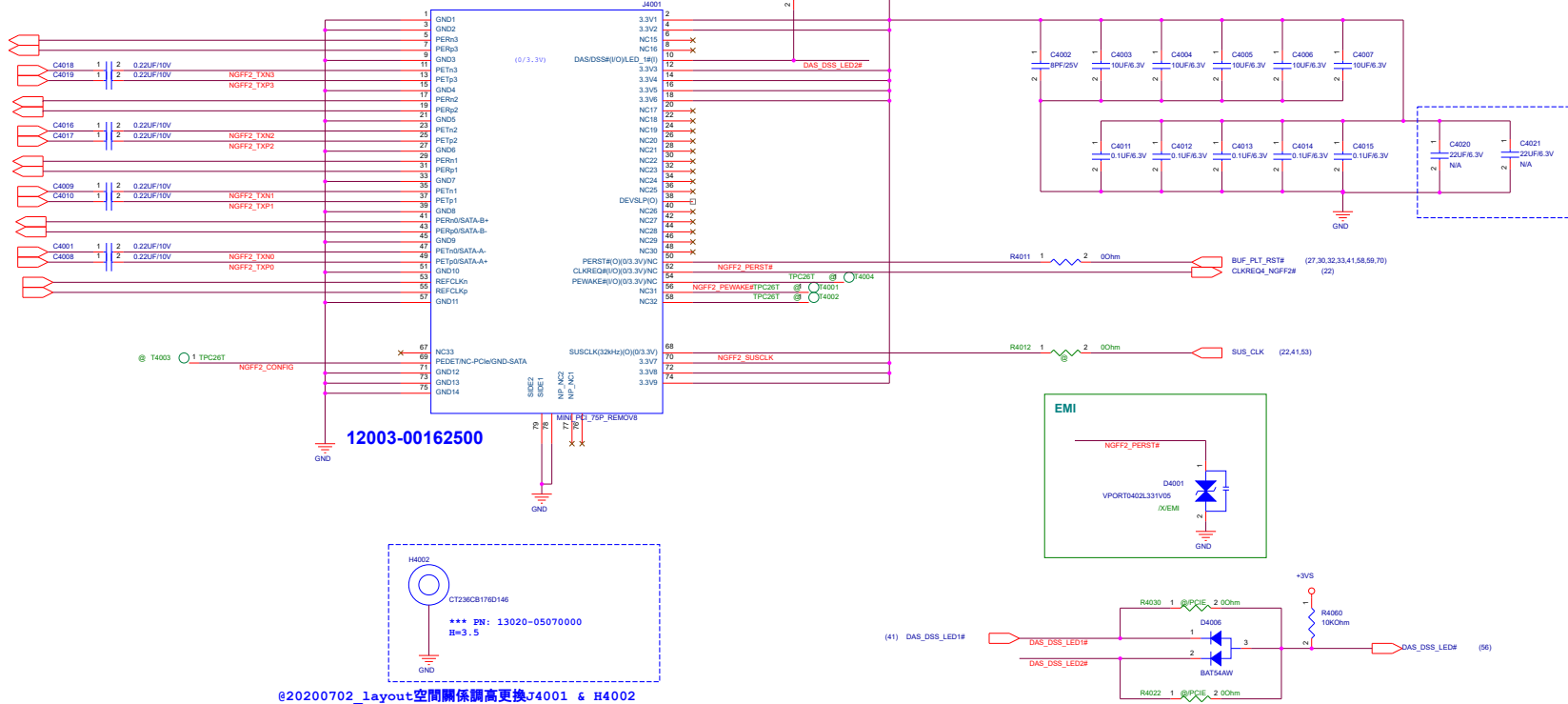
PCIE6  
NGFF2 PCIE Lane1

- (21) PCIE6\_RXN\_NGFF2\_L1
- (21) PCIE6\_RXP\_NGFF2\_L1
- (21) PCIE6\_TXN\_NGFF2\_L1
- (21) PCIE6\_TXP\_NGFF2\_L1

PCIE5  
NGFF2 PCIE Lane0

- (21) PCIE5\_RXN\_NGFF2\_L0
- (21) PCIE5\_RXP\_NGFF2\_L0
- (21) PCIE5\_TXN\_NGFF2\_L0
- (21) PCIE5\_TXP\_NGFF2\_L0

- (22) CLK0\_PCIE\_NGFF2#
- (22) CLK1\_PCIE\_NGFF2





<Variant Name>

Project Name		Rev
ASUS		R2.1
Title : CB AU6465		
Size	Dept.: NB1-RD3EE2	Engineer: Huang
C	Date: Tuesday, December 29, 2020	Sheet 40 of 102

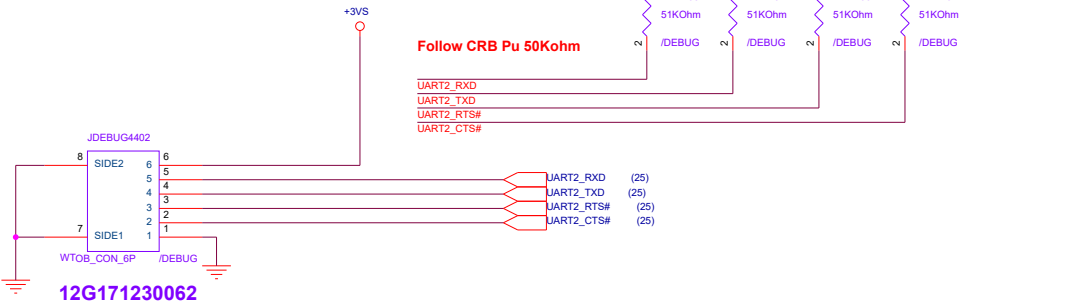


<Variant Name>

		<b>Title :</b> XDD_HDD & ODD CON	
ASUSTeK COMPUTER		<b>Engineer:</b> EE	
Size A	Project Name GX502GX		Rev 1.0
Date: Tuesday, December 29, 2020		Sheet 42	of 102


		Project Name <b>UX482</b>		Rev  R0.1
Title : <b>CB-****</b>				
Size  C	Dept.: <b>NB1-RD3EE2</b>		Engineer:	<b>EE</b>
Date: <b>Tuesday, December 29, 2020</b>			Sheet <b>43</b>	of <b>102</b>

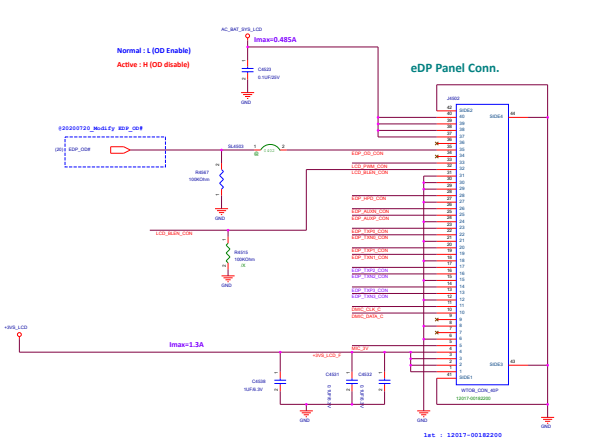
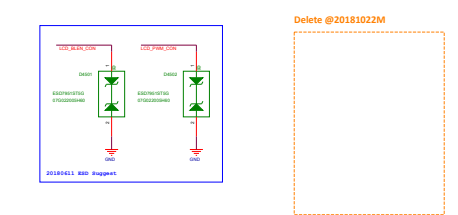
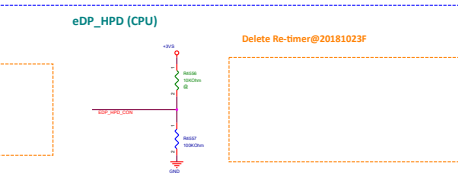
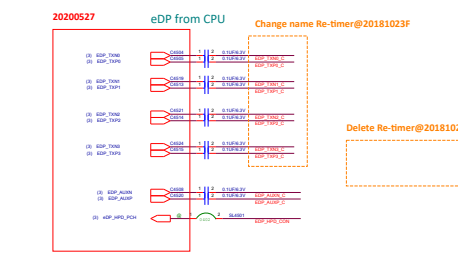
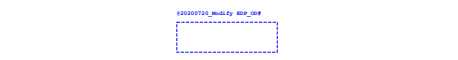
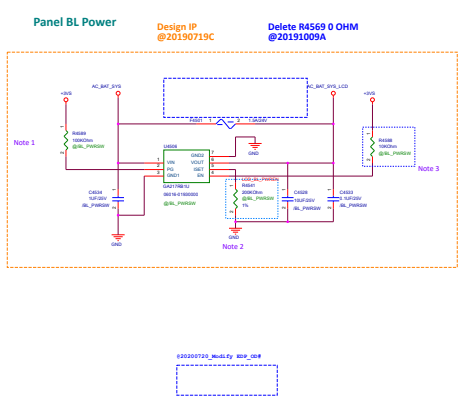
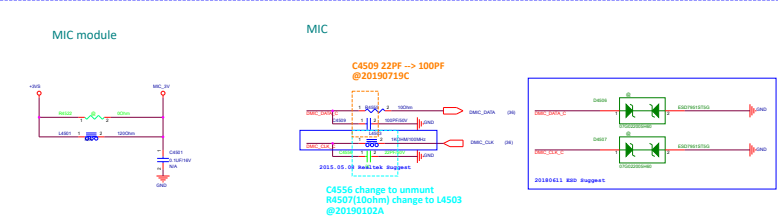
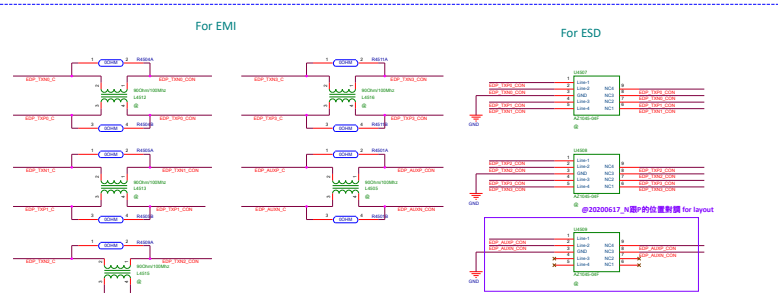
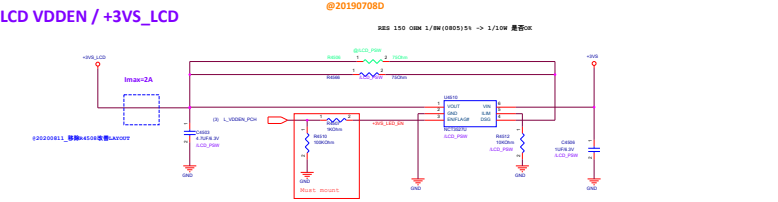
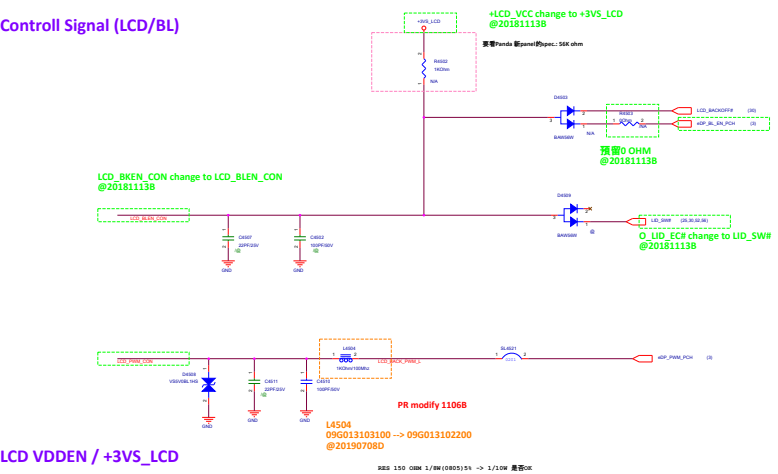
UART Debug card




Jigboard4 debug guide  
DIP SW to 0000 : BIOS Flash  
DIP SW to 0010 : Keyboard CONN Port80  
DIP SW to 1000 : SMBUS CONN Port80 & BIOS DUMP (by Postcode monitor)

<Core Design>


		Title : <b>DEBUG_LPC</b>	
ASUSTeK COMPUTER		Engineer: <b>EE</b>	
Size <b>B</b>	Project Name <b>GX502GX</b>		Rev <b>1.0</b>
Date: <b>Tuesday, December 29, 2020</b>		Sheet <b>44</b> of <b>102</b>	





		Project Name		Rev
		<b>UX482</b>		R0.1
<b>Title :</b> <b>CRT_D-Sub</b>				
Size	<b>Dept.:</b> <b>NB1-RD3EE2</b>		<b>Engineer:</b>	<b>EE</b>
B				
Date: <b>Tuesday, December 29, 2020</b>			Sheet	<b>46</b> of <b>102</b>

~Variant Name~

		Project Name <b>UX482</b>		Rev <b>R0.1</b>
Title : <b>Display Port</b>				
Size <b>C</b>	Dept.: <b>MSI-PD3002</b>		Engineer: <b>EE</b>	
Date: <b>Tuesday, December 29, 2020</b>			Sheet <b>47</b>	of <b>102</b>

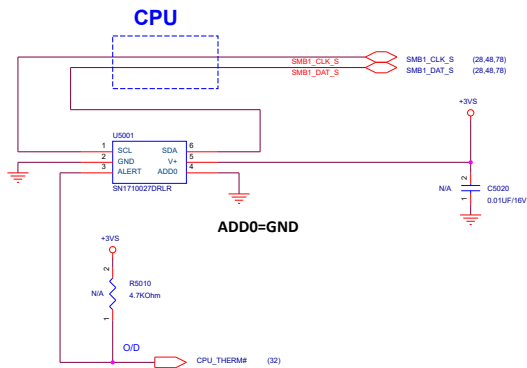


## Thermal Sensor : SN170027

**ALERT/SDA/SCL: Open-drain output; pullup resistor 5Kohm**

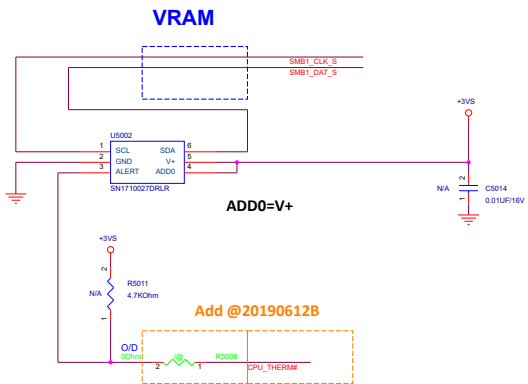
**Pin function Supply voltage.: 1.62 V to 3.6 V**

@20200728\_Modify thermal Del. 0 ohm



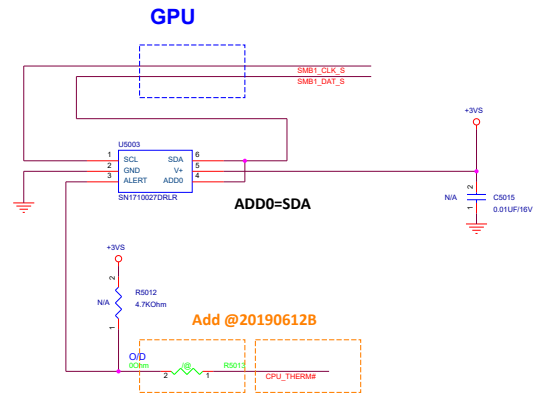
### Near CPU

SMBUS addr=10010000 (90)



### Near VRAM

SMBUS addr=10010001 (91)

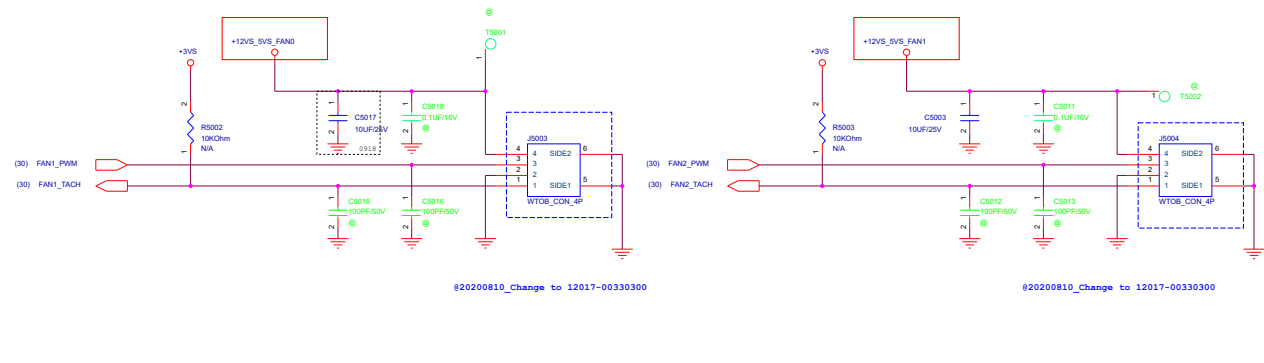


Near GPU

SMBUS addr=10010010 (92)

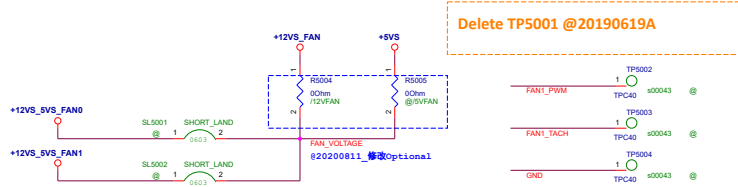
## CPU&GPU FAN

**Note : connector and power are by project design**



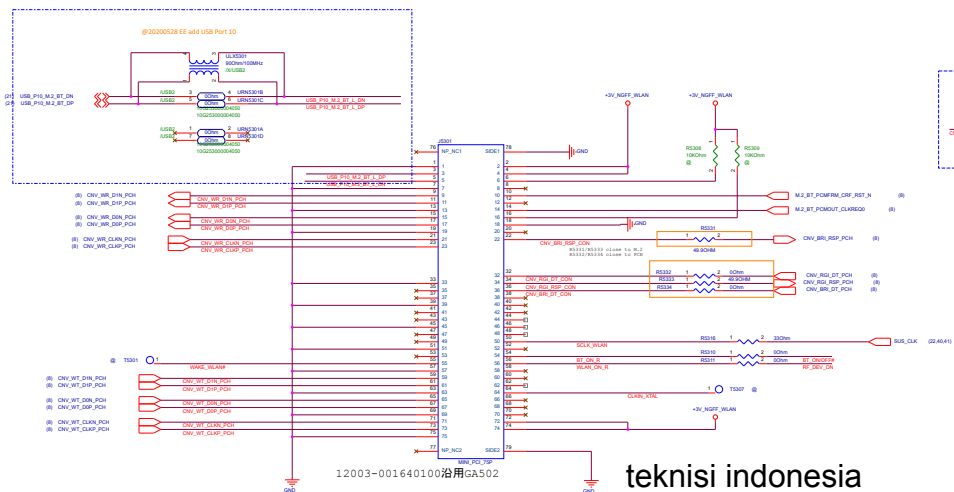
**ADD0:** Address select. Connect to GND, SDA, SCL, or V+

DEVICE TWO-WIRE ADDRESS	ADD0 PIN CONNECTION	Output
1001000 <b>90</b>	Ground	CPU
1001001 <b>91</b>	V+	VRAM
1001010 <b>92</b>	SDA	GPU
1001011 <b>93</b>	SCL	



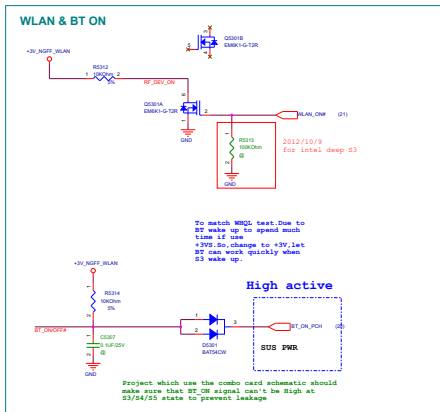


## NGFF M.2 TYPE\_E-KEY WIFI



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## @20200611\_del WLAN\_Wake# Control for RF



## Screw Hole

12003-01071400

Screw Hole 4.0x4.0mm (Hole 4.0x4.0mm)



20200707 Rex 新增

## Main Board

## WLAN PWR\_+3V\_NGFF\_WLAN (Non-5CT)

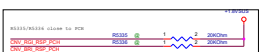
Support ASUS Open Cloud Computing (AOCConnect)

WLAN PWR to +3VSD5



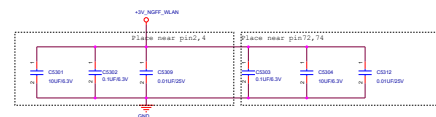
Remove WLAN and LAN power switch circuit

2019.11.19



12003-001640100 通用GA502

## WLAN NGFF\_WLAN bypass capacitor



©Core Design



Project Name

**UX482**

Rev

R0.1

**Title :**      **G-Sensor**

Size

**B**

**Dept.:**      **NB1-RD3EE2**

**Engineer:**      **EE**

Date: **Tuesday, December 29, 2020**

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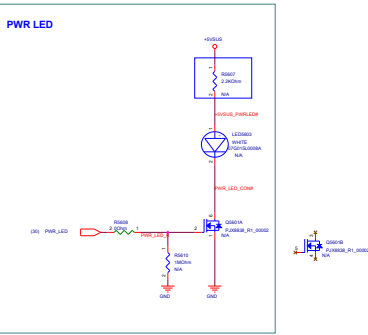


@20181013C

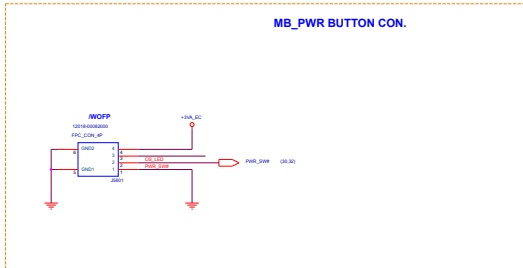
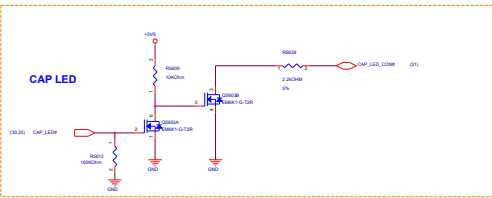
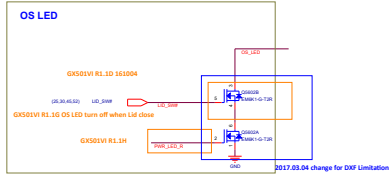
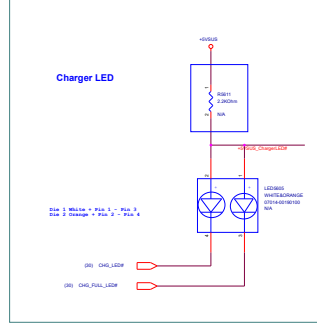
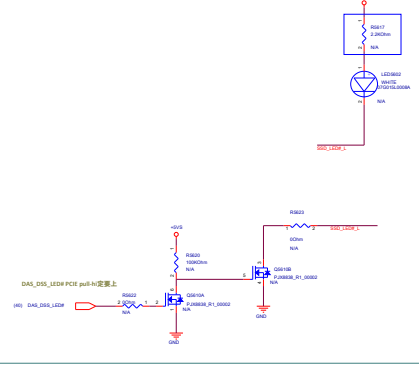
PWR LED

PCIE SSD LED

Charger LED



PCIE SSD LED



KB connector change to P.31  
@20190731C

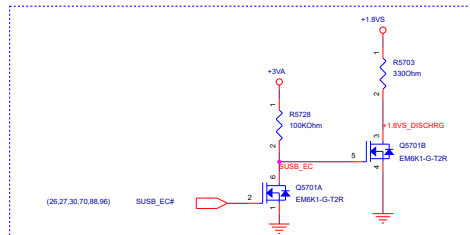
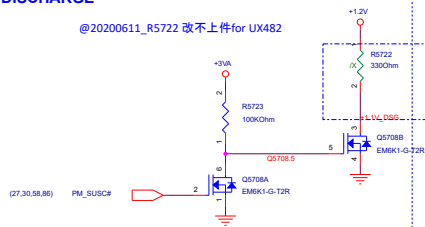
Change to monst @ 20181129A

FP No	GA502 FP Pwrbtn	GA502 小板	GA502 小板 pin No
10	LED+	LED+	4
9	LED-	LED-	3
8	PWRBTN	PWRBTN	2
7	GND	GND	1
6	USB_D-	-	-
5	USB_D+	-	-
4	GND	-	-
3	SSO	-	-
2	ATC	-	-
1	RESETn	-	-

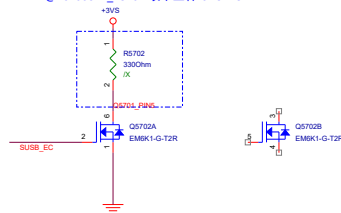
Justin : Removed no used Discharge circuit  
1.8V, VCCIO, +5VS load switch already build in 180~260 ohm discharge function

## +1.1V DISCHARGE

@20200611\_R5722 改不上件for UX482



@20200611\_R5702 改不上件for UX482

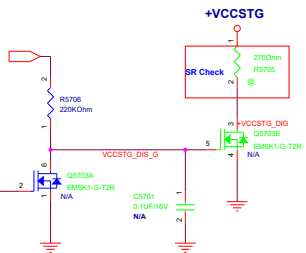


## +VCCSTG

(26) VCCSTG\_EN\_12V

Use 12VS\_GATE and VCCSTG\_EN\_12V  
for board optimization

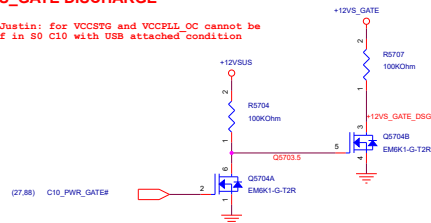
+12VS\_GATE



VCCSTG should have a discharge circuit recommended nominal Discharge => 300 to 500.  
And activated when the VCCSTG load switch is disabled

## +12VS\_GATE DISCHARGE

R1.1B Justin: for VCCSTG and VCCPLL\_OC cannot be  
cut off in S0 C10 with USB attached condition

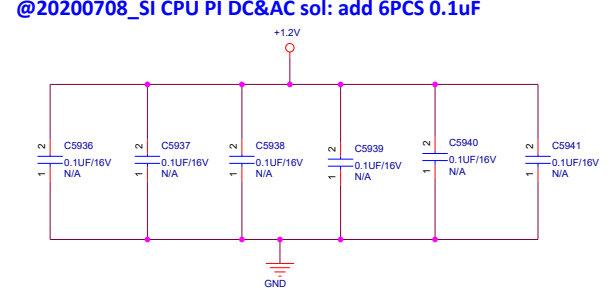
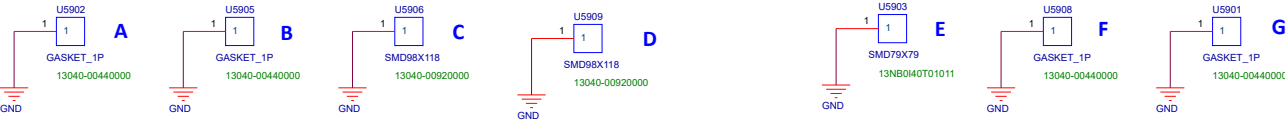


<<Variant Name>>

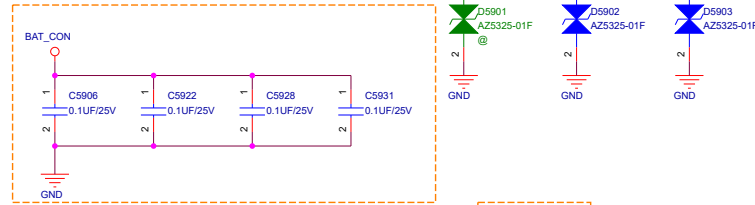
ASUS		Project Name	Rev
Title : DSG_Discharge		UX482	R0.1
Size	Dept.: N81-RD3EE2	Engineer: EE	
Date: Tuesday, December 29, 2020	Sheet	57	of 102



# @20201021\_Modify SMT EMI GASKET

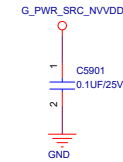
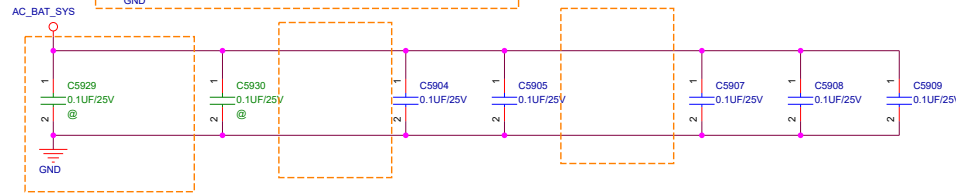
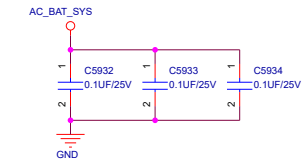


## EMI request @20181026A

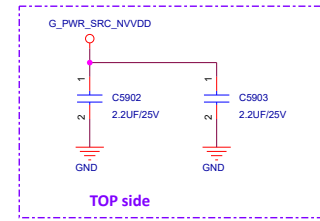


將U6904, U6908(改裸銅), U6905(改裸銅) 移除  
@20181122C

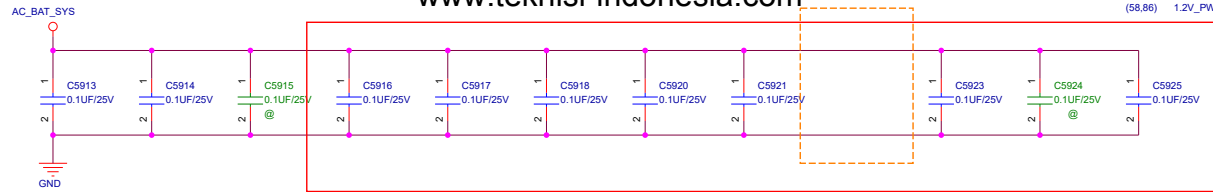
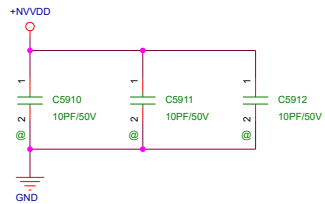
## 2017/04/05 EMI



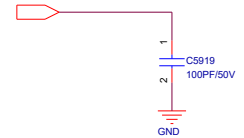
## 4/2 for EMI



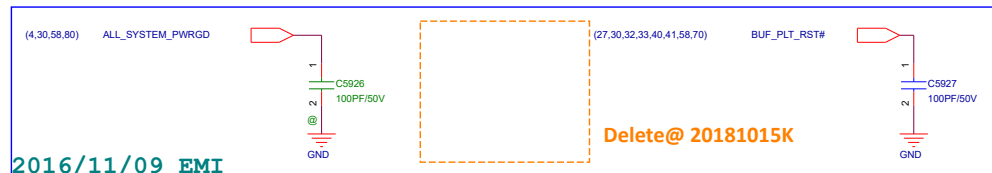
## 2016/07/27 EMI



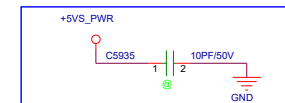
GX501VI 1.1H



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## 2016/11/09 EMI



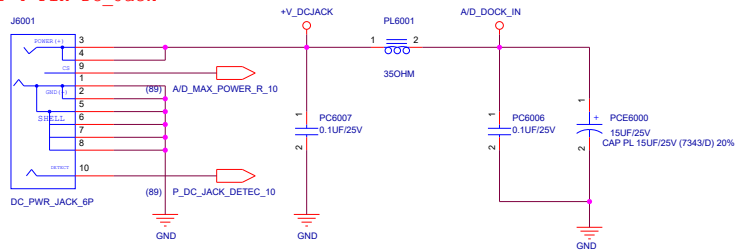
<Core Design> 2017.05.02 EMI Reserve

ASUS		Title : OTH_EMI	
ASUSTek COMPUTER		Engineer: EE	
Size B	Project Name GX502GX	Rev 1.0	
Date: Tuesday, December 29, 2020	Sheet 59	of	102

DC-IN Connector

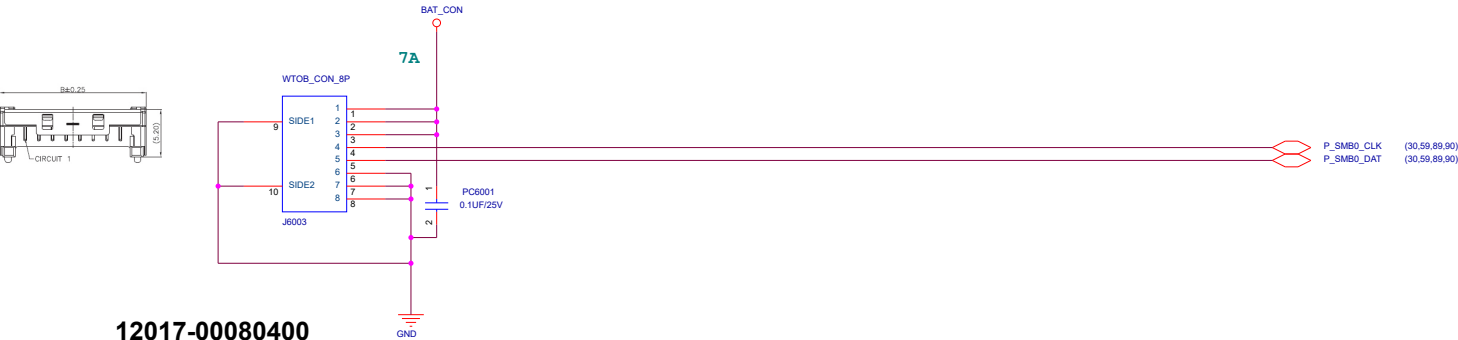
DC Jack使用請詢用River\_Hsu

New 6 Phi 4 Pin DC\_Jack



J6001	3.4CH	1.55CH
	12033-00020200	12033-00020300

Battery Connector



12017-00080400

Note:Battery Connector 正確性與BAT1\_IN\_OC#是否預留！



Project Name

**UX482**

Rev

R0.1

**Title :**

Size

C

**Dept.:** NB1-RD3EE2**Engineer:** EE

Date: Tuesday, December 29, 2020

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**Title :**

**I/O board(1-1)\_CR\_RTS5139**

**ASUSTeK COMPUTER**

**Engineer:**

**EE**

Size

Project Name

Rev

**A**


**GX502GX**

**R1.2**

Date: **Tuesday, December 29, 2020**


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<Variant Name>

		Project Name <b>UX482</b>		Rev  R0.1
Title : <b>NFC</b>				
Size  C	Dept.: <b>NB1-RD3EE2</b>		Engineer:	<b>EE</b>
Date: <b>Tuesday, December 29, 2020</b>			Sheet <b>63</b>	of <b>102</b>

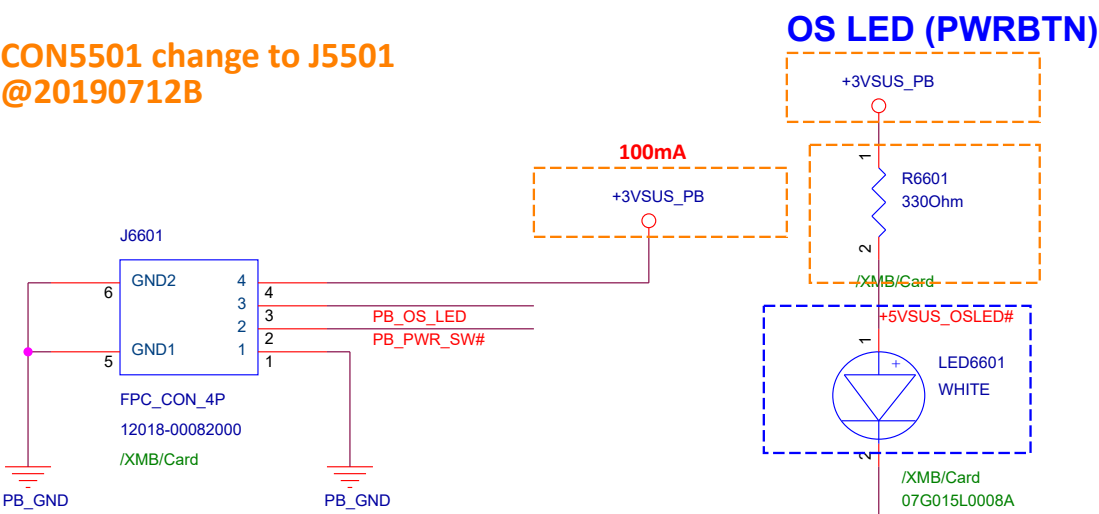


BOM

		Project Name	Rev
		UX482	RD.1
Title :			
Size	Dept.:	Engineer:	
B	NB1-RD3EE2	EE	
Date:	Tuesday, December 29, 2020	Sheet	64 of 102

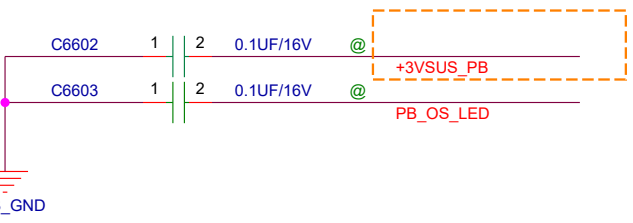
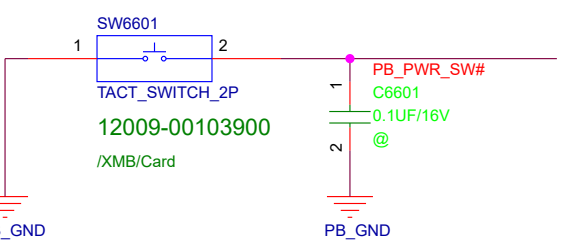


CON5501 change to J5501  
@20190712B

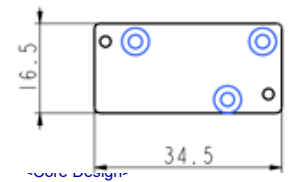
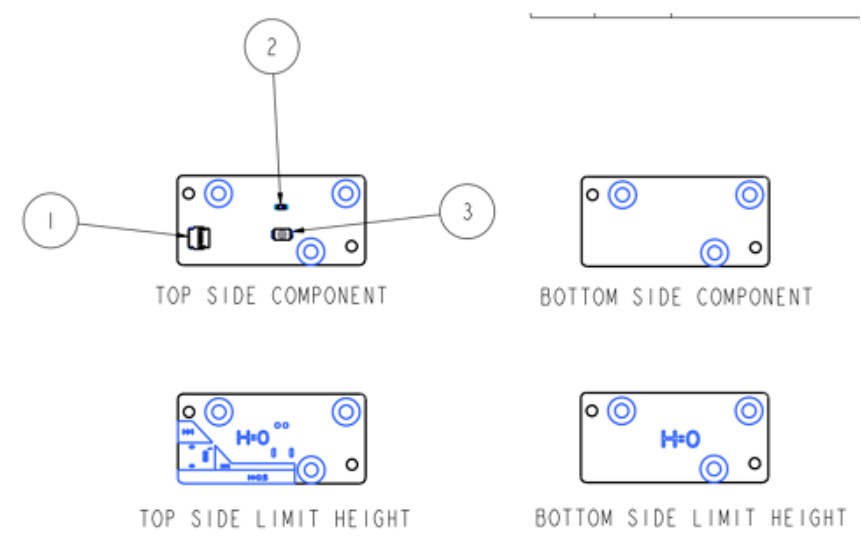
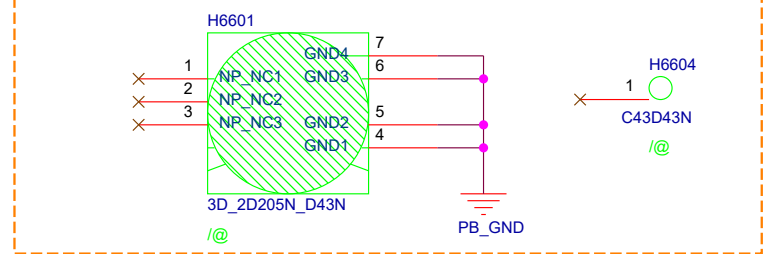



@20200813 Power Key LED 换白光 07G015L0008A  
**+5VSUS\_PB --> +3VSUS\_PB**  
**R5510 750 OHM --> 330 OHM**  
**@20190708A**

POWER button



Change @20181026B




		Title : <b>IO Con. to MB</b>	
ASUSTeK COMPUTER		Engineer: <b>EE</b>	
Size <b>A</b>	Project Name <b>GX502GX</b>		Rev <b>1.0</b>
Date: <b>Tuesday, December 29, 2020</b>		Sheet <b>66</b> of <b>102</b>	

Del.@20201215

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<Variant Name>

		Title : KBC_KB & TP	
ASUSTeK COMPUTER		Engineer: EE	
Size C	Project Name GM501		Rev R1.0
Date: Tuesday, December 29, 2020		Sheet 67 of 102	



Project Name

**UX482**

Rev

R0.1

**Title :**

Size

B

**Dept.:** NB1-RD3EE2**Engineer:** EE

Date: Tuesday, December 29, 2020

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<Variant Name>

Title

<Title>

Size

A

Document Number

G512LI

Rev

R1.0

Date:

Tuesday, December 29, 2020

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<Variant Name>

Title

<Title>

Size

A

Document Number

G512LI

Rev

R1.0

Date:

Tuesday, December 29, 2020

Sheet

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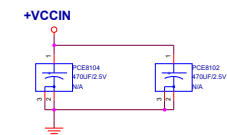
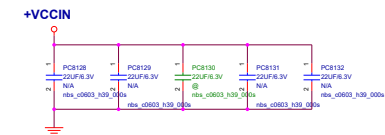
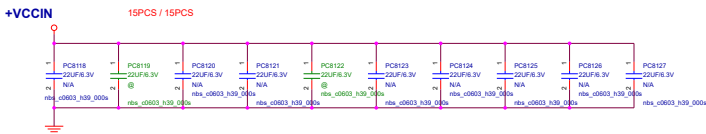
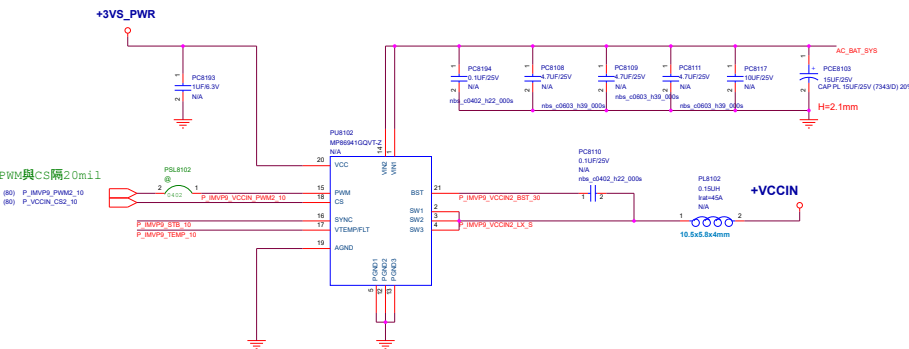
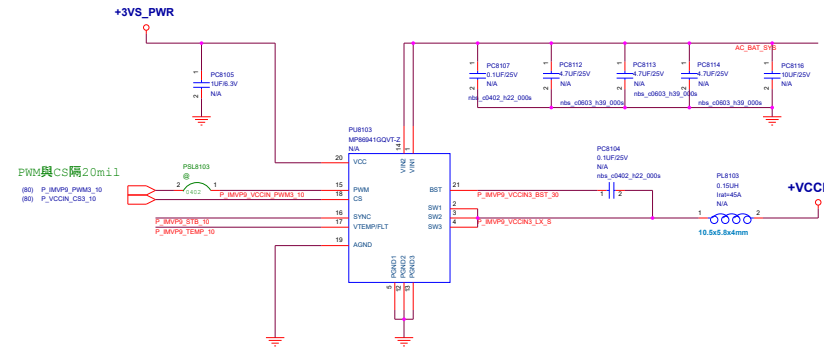
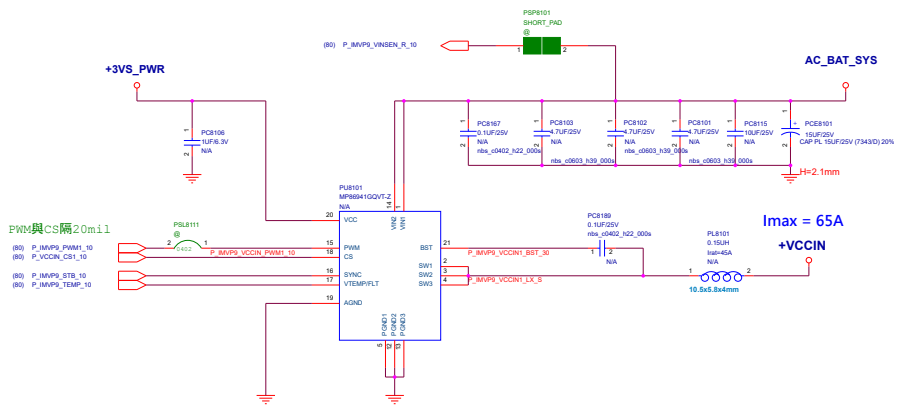
102



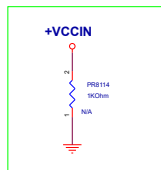
**ICCMAX=65A**



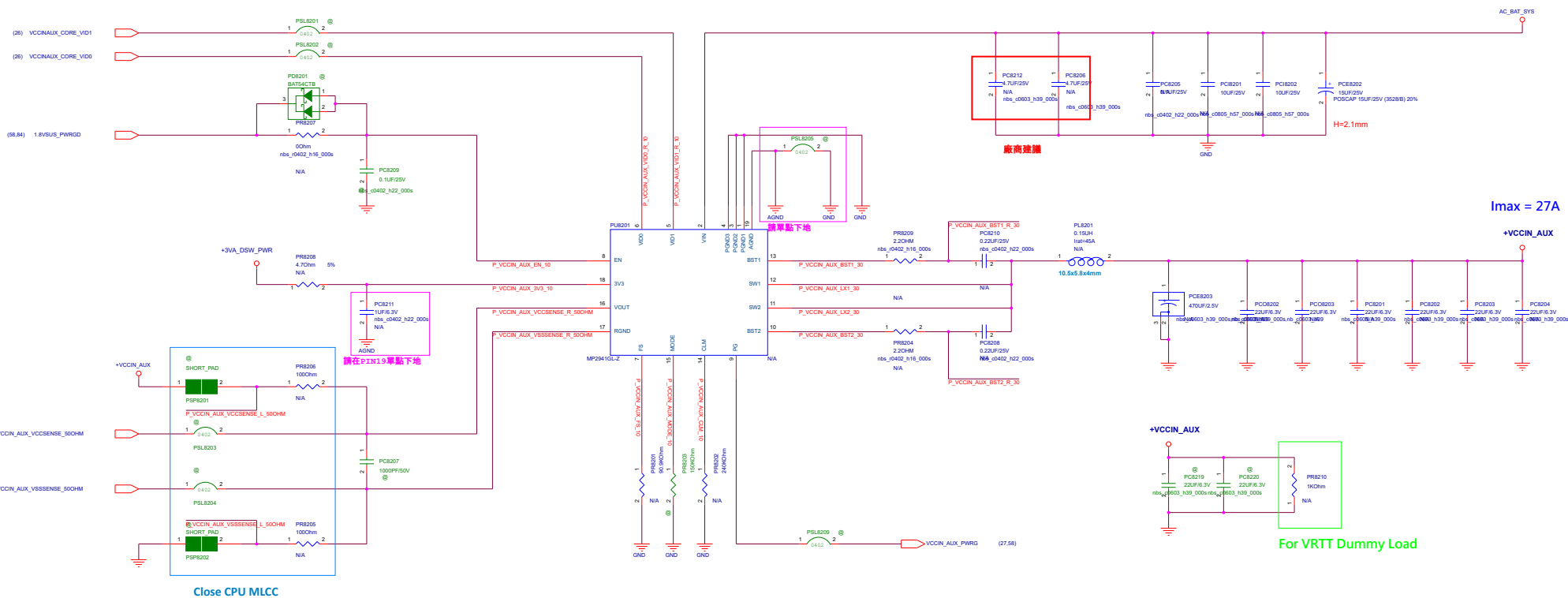
# TGL IMVP9 (2) Power [For CPU]



For VRTT Dummy Load



### TGL IMVP9 (3) Power [For CPU]



<Variant Name>



Project Name

**UX482**

Rev

**R0.1**

**Title :**     **POWER**

Size

**Custom**

**Dept.:**     **NB1-RD3EE2**

**Engineer:**     **Andy**

Date: **Tuesday, December 29, 2020**

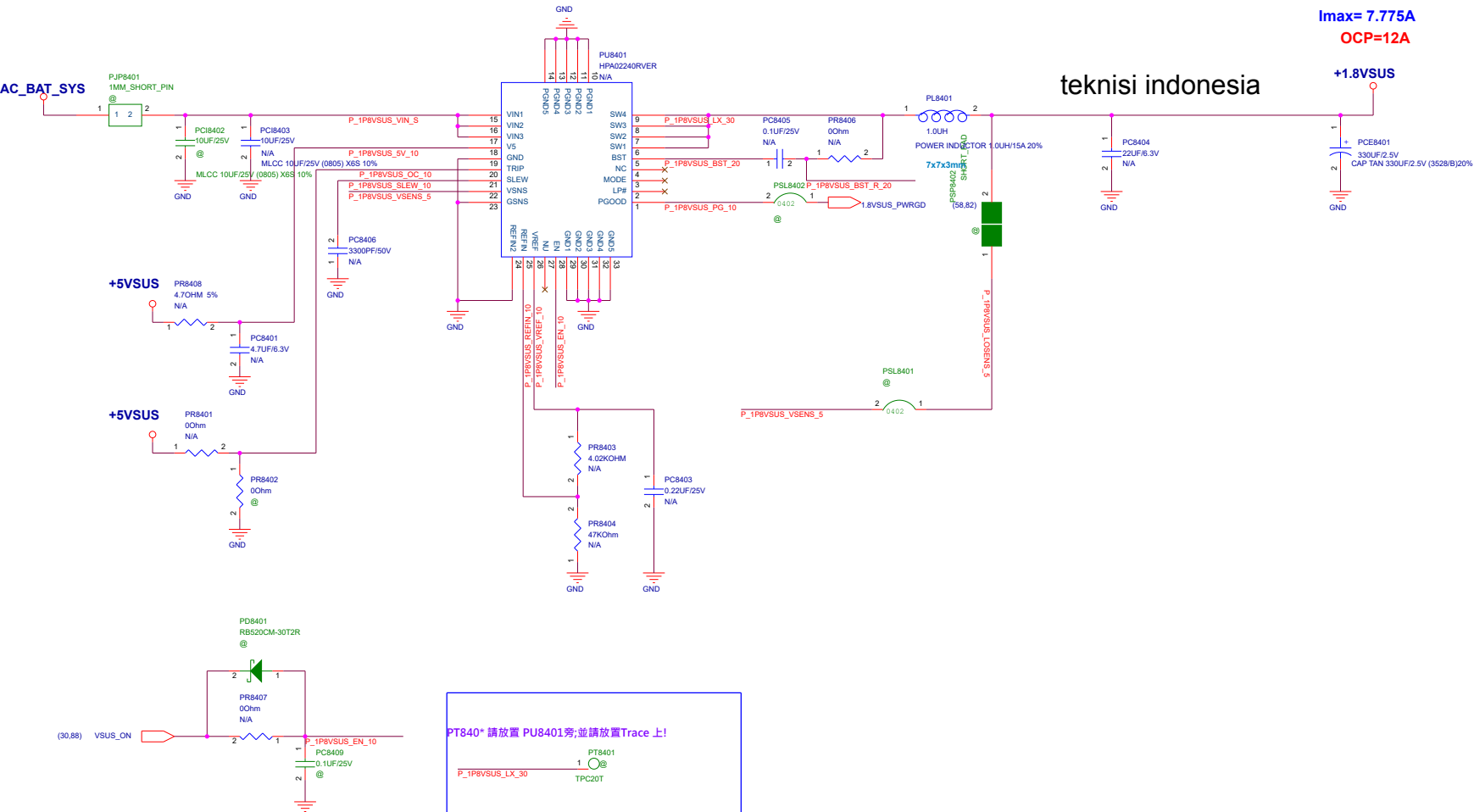
Sheet

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# +1.8VSUS [For PCH]



<Variant Name>

<b>ASUS</b>		Project Name	Rev
		Project Name	R1.0
Title : PW_+1.8VSUS			
Size	Dept.:	Engineer:	Power RD
A3	NB Power team		
Date: Tuesday, December 29, 2020	Sheet	84	of 102

<Variant Name>



Project Name

**UX482**

Rev

**R0.1**

**Title :**     **POWER**

Size

**Custom**

**Dept.:**     **NB1-RD3EE2**

**Engineer:**     **Andy**

Date: **Tuesday, December 29, 2020**

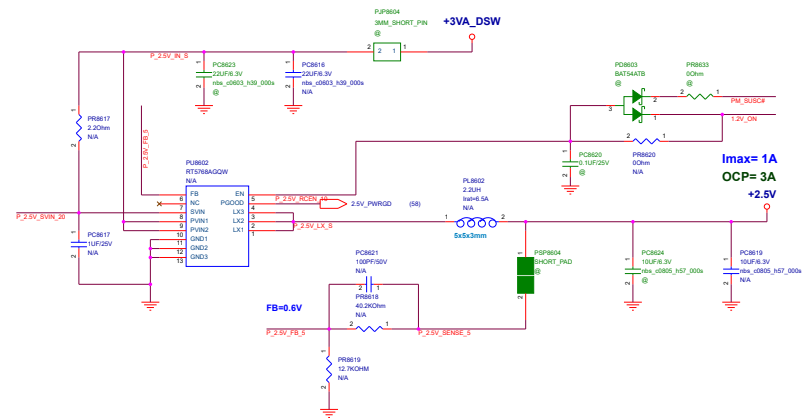
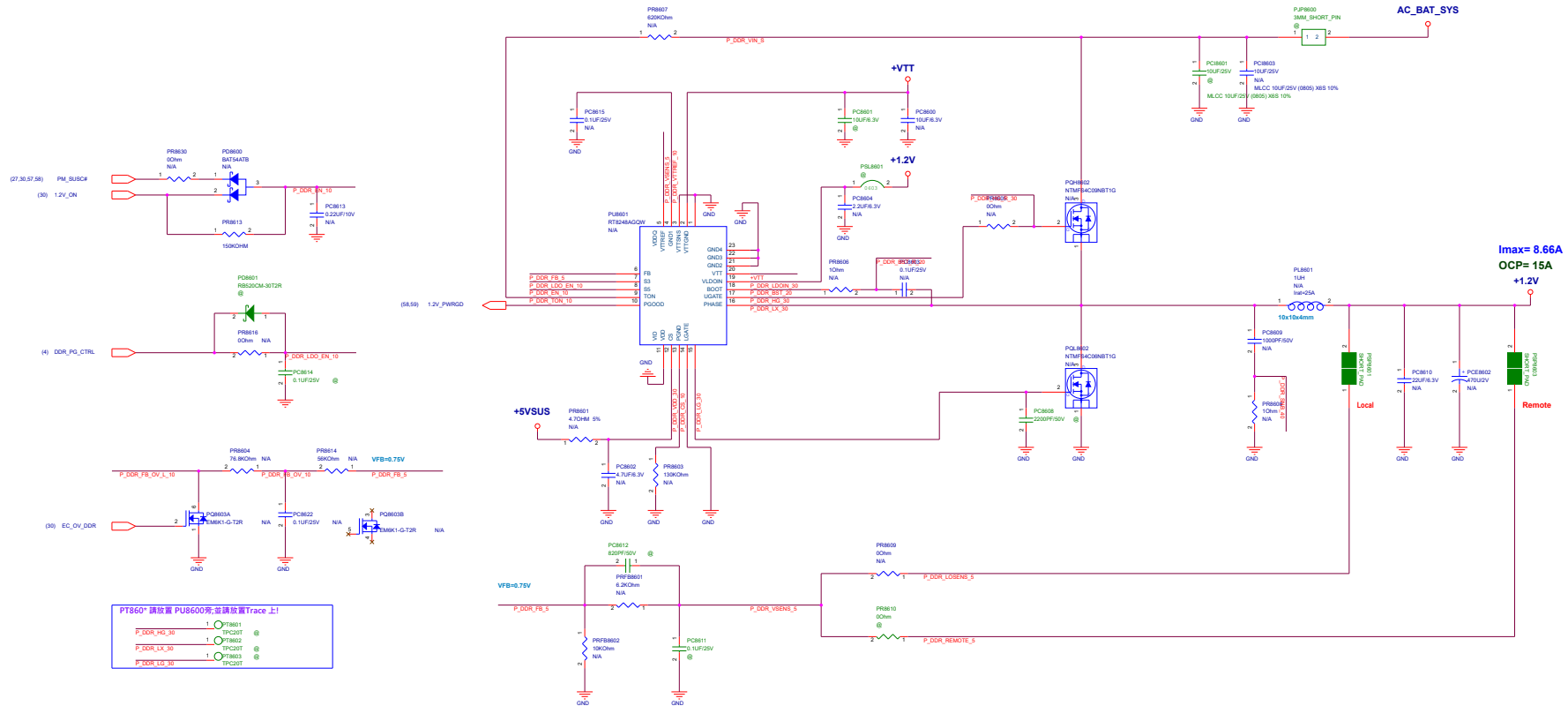
Sheet

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of

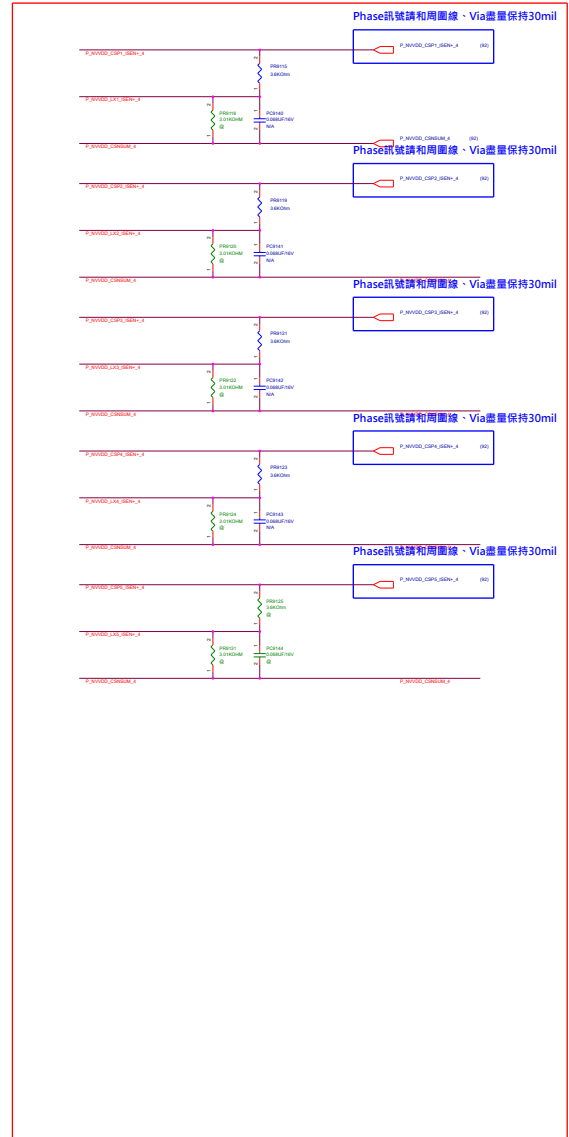
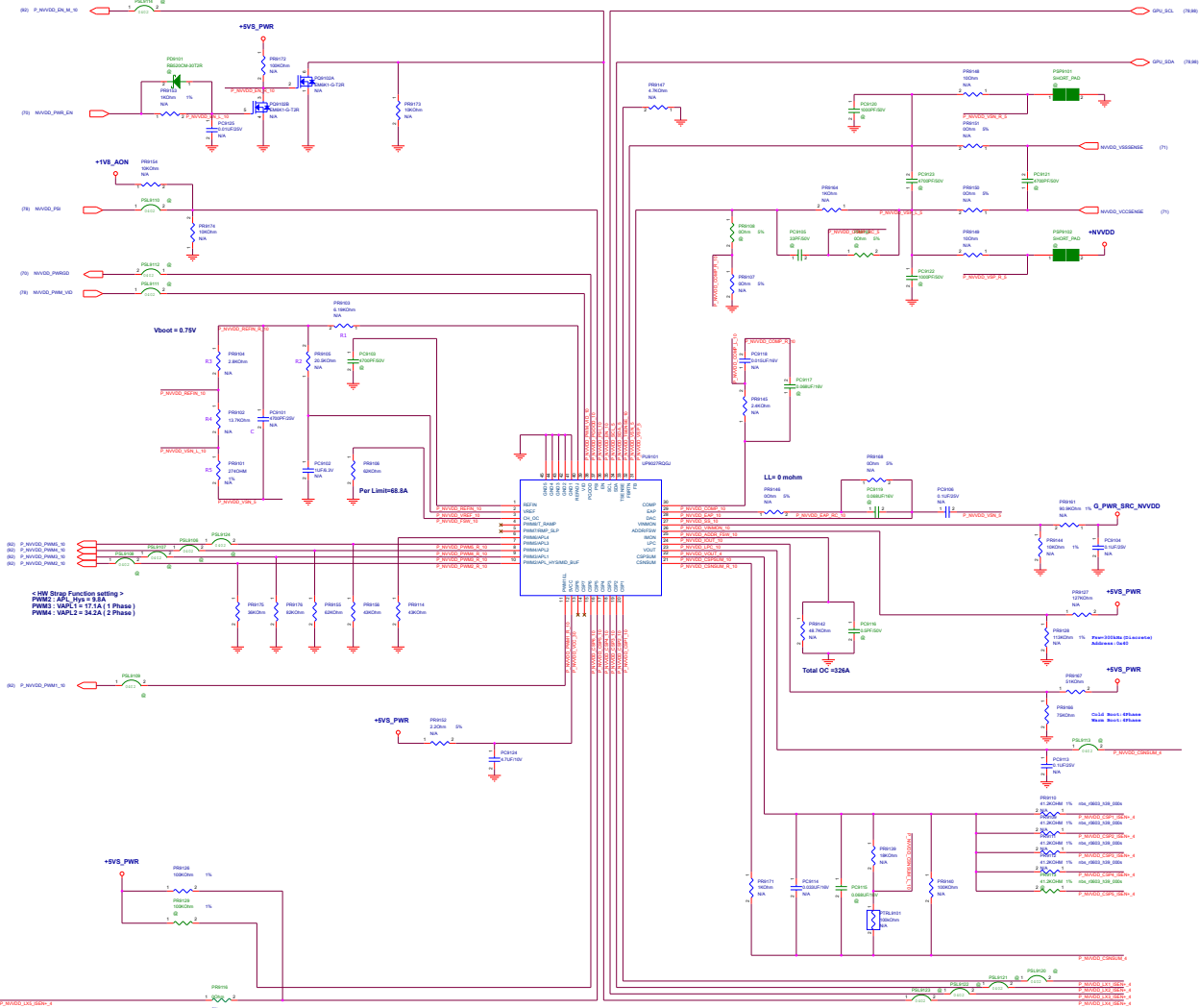
**102**

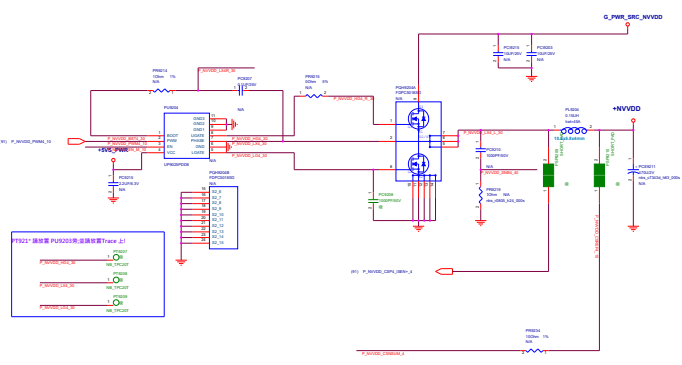
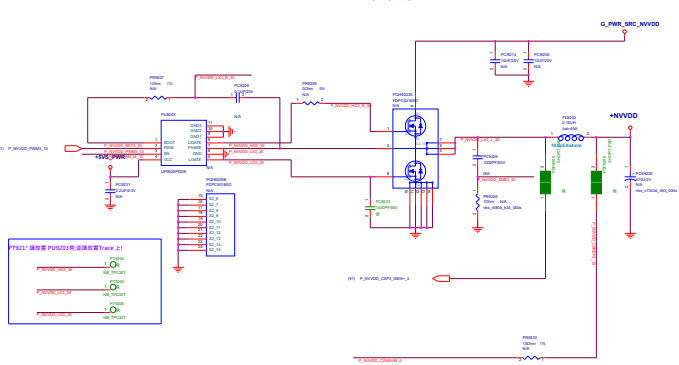
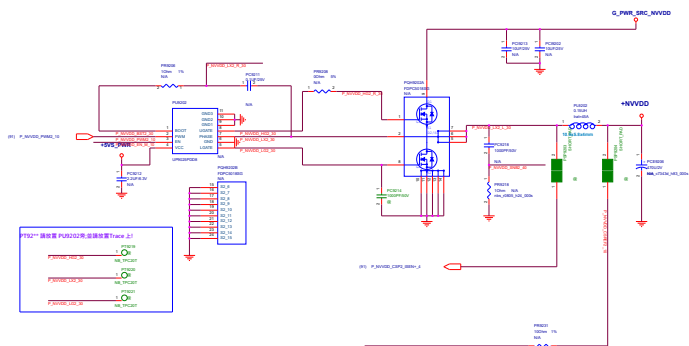
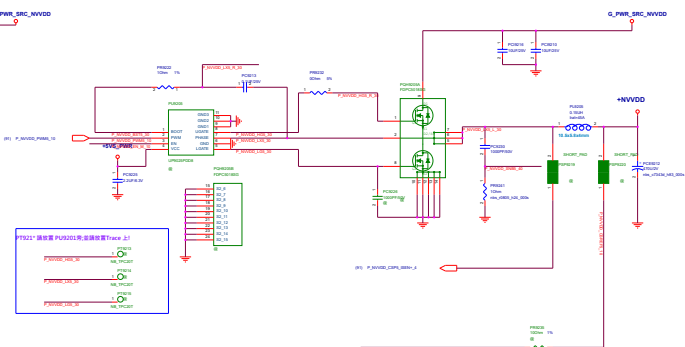
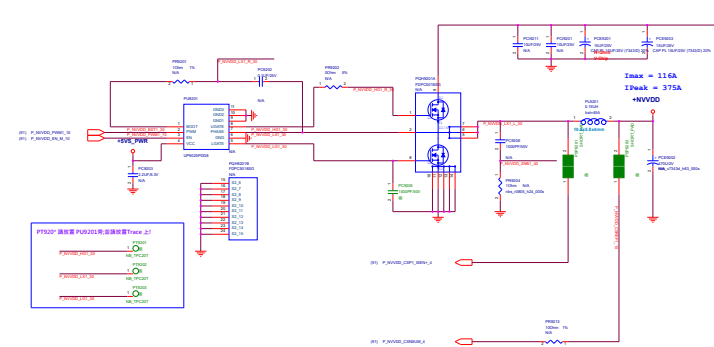
# +1.2V / +VTT / +2.5V[For Memory]

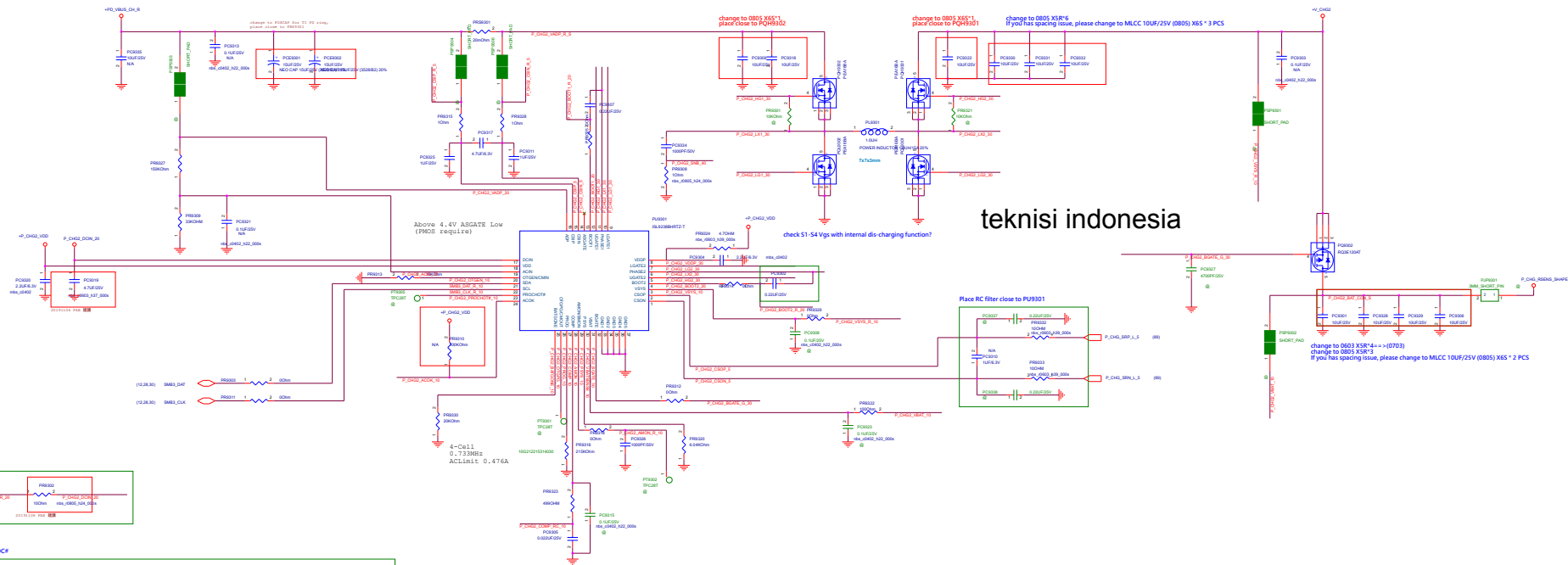






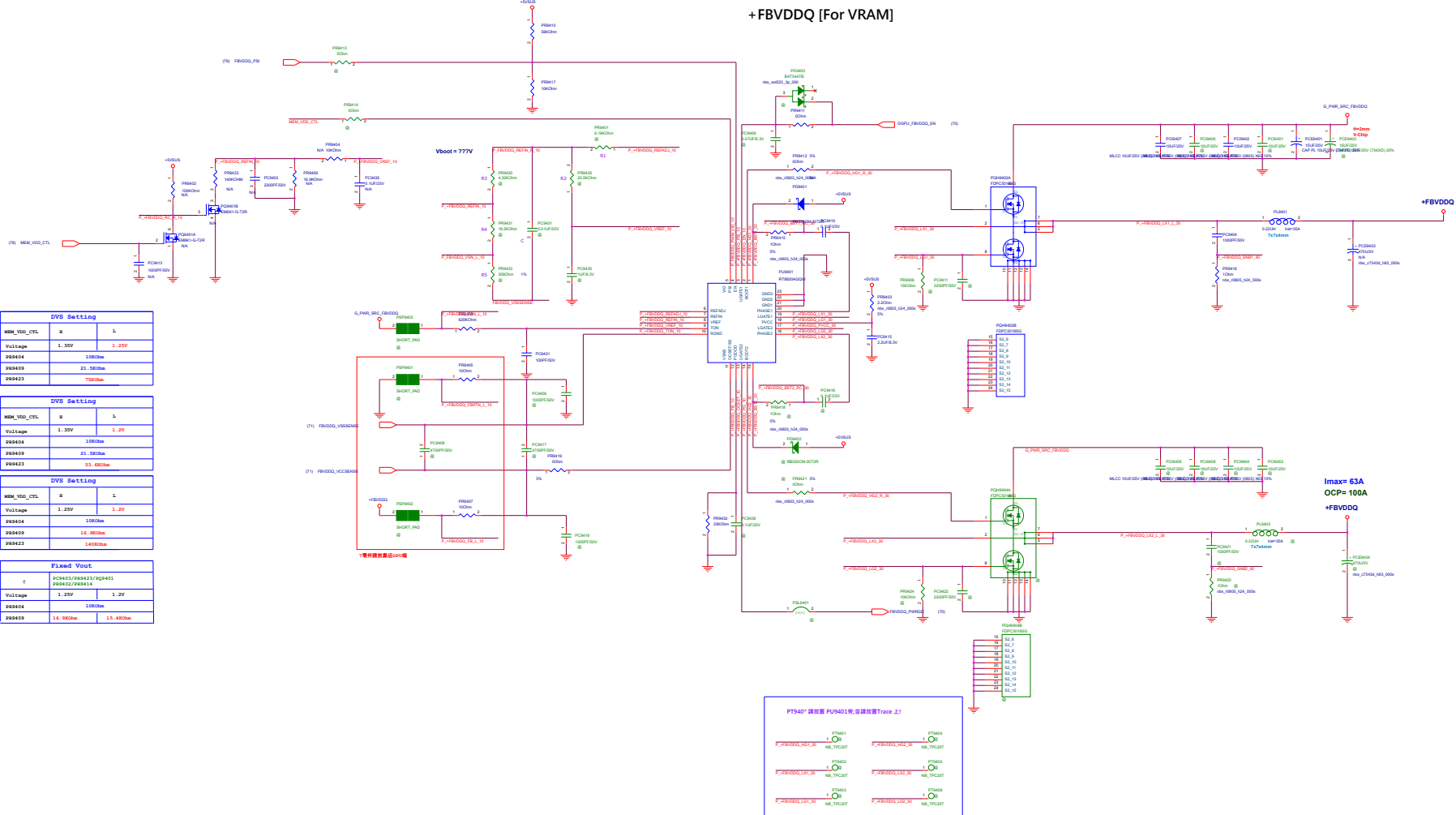






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# +FBVDDQ (For VRAM)



Copyright Notice

<Variant Name>



Project Name

**UX482**

Rev

**R0.1**

**Title :**     **POWER**

Size

**Custom**

**Dept.:**     **NB1-RD3EE2**

**Engineer:**     **Andy**

Date: **Tuesday, December 29, 2020**

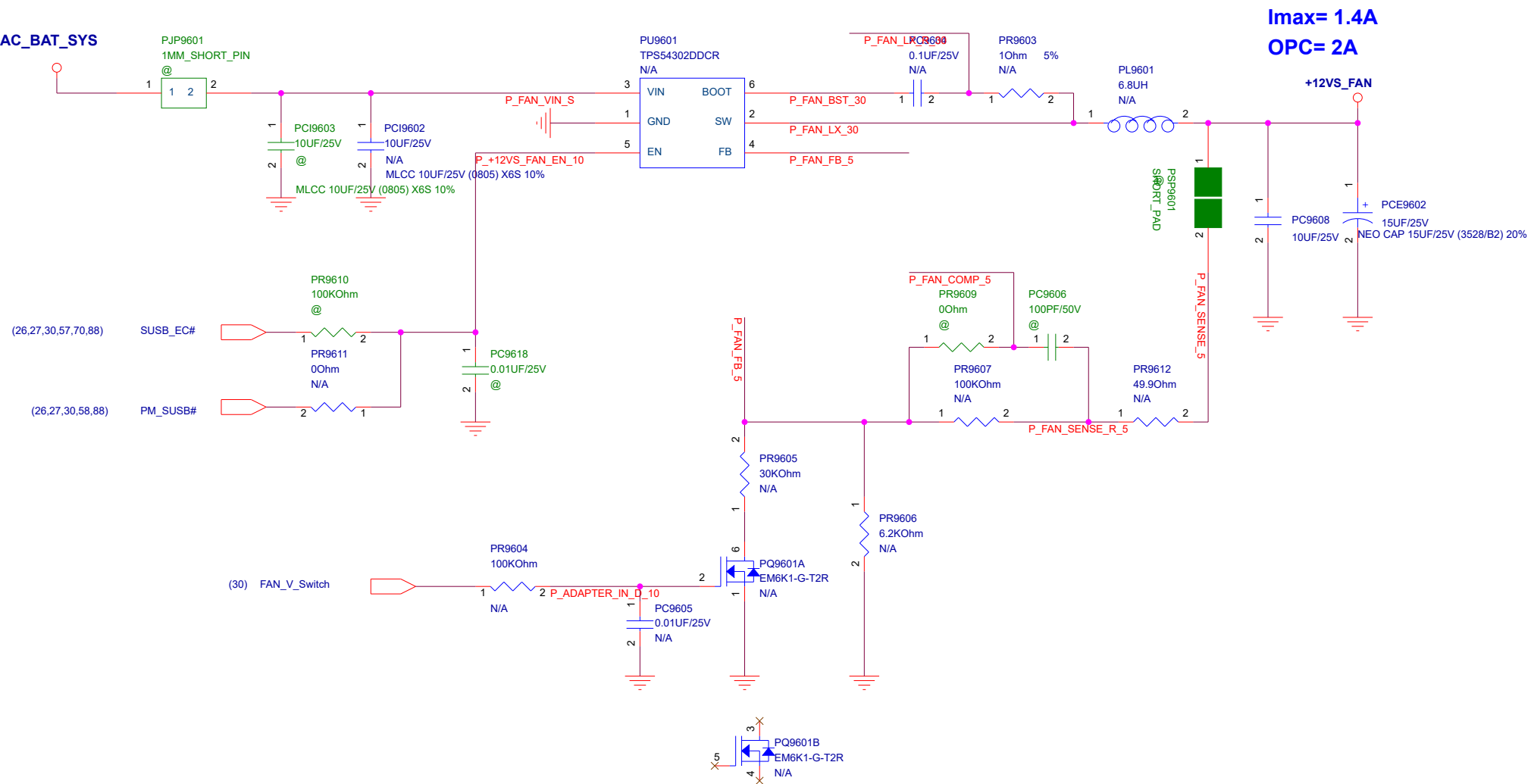
Sheet

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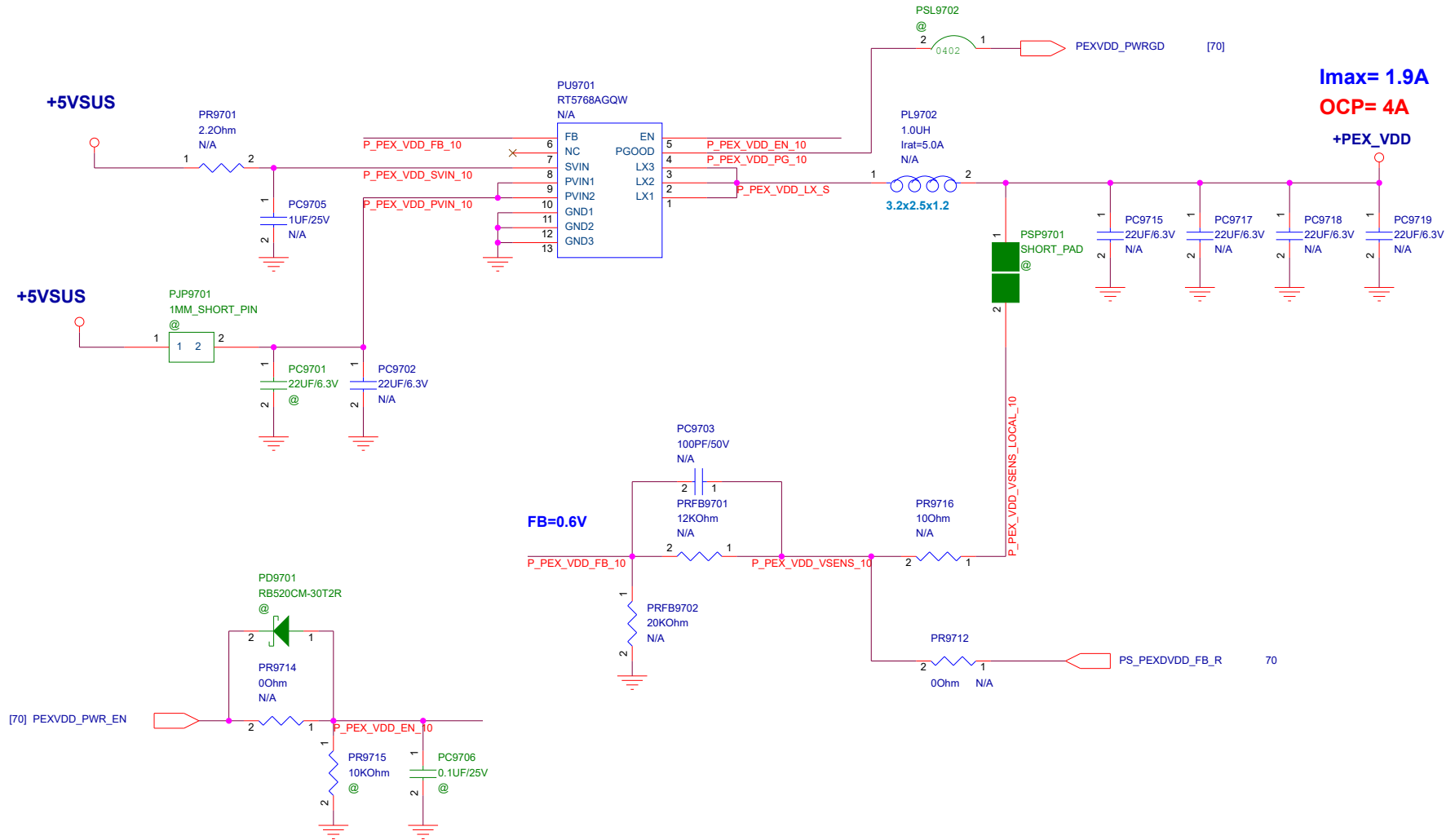
## +12VS\_FAN [For FAN]



<Variant Name>

		Project Name <b>Project Name</b>		Rev R1.0	
<b>Title :</b> <b>PW_+12VS_FAN</b>					
Size A4		<b>Dept.:</b> <b>NB Power team</b>		<b>Engineer:</b> <b>Power RD</b>	
Date: <b>Tuesday, December 29, 2020</b>				Sheet <b>96</b> of <b>102</b>	

# PEX\_VDD [For GPU]



<Core Design>

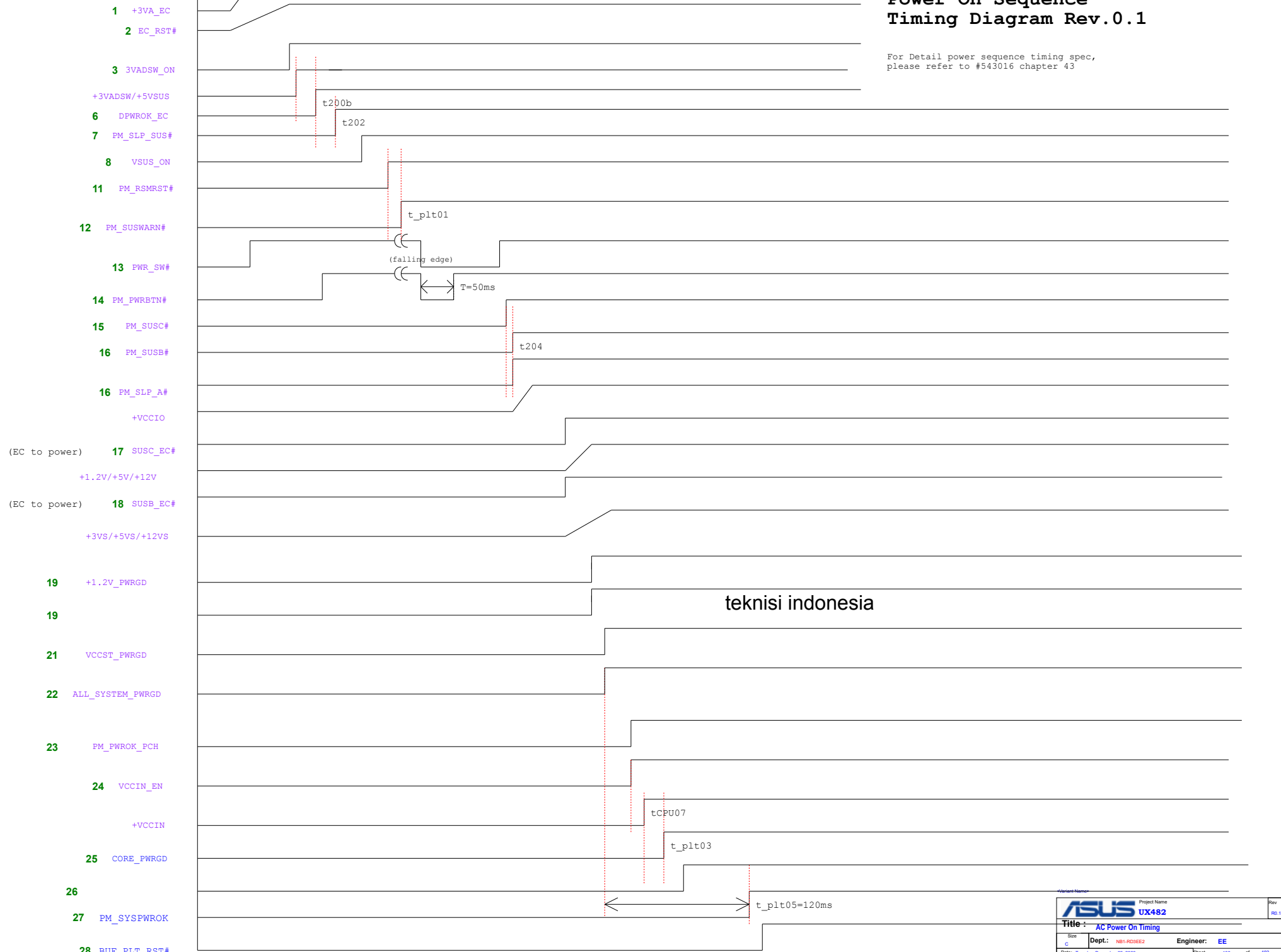
		Project Name	Rev
<b>Title :</b> PW_+PEX_VDD		Project Name	R1.0
Size A4	Dept.: NB Power team	Engineer: Power RD	
Date: Tuesday, December 29, 2020	Sheet 97	of 102	



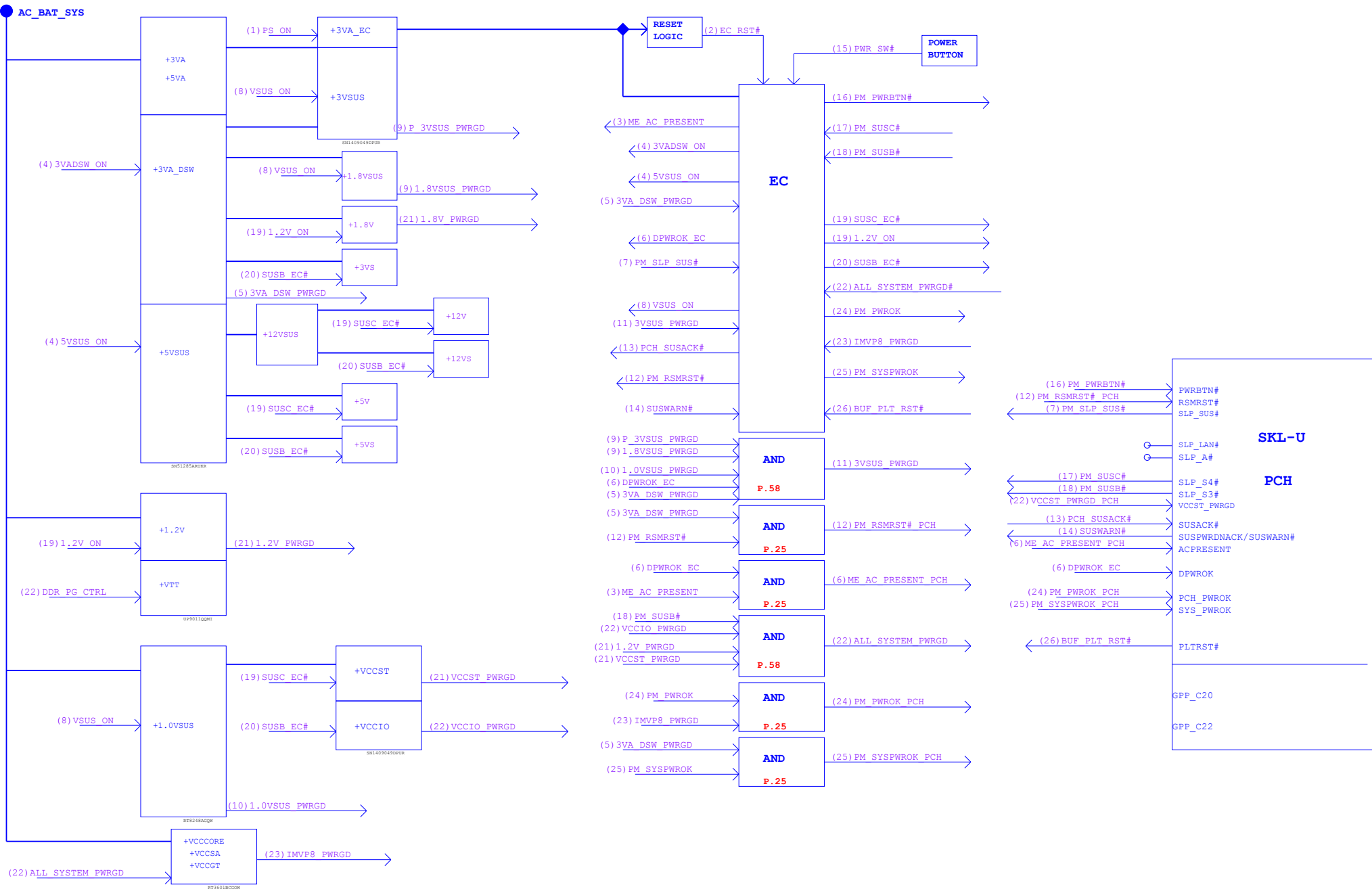


# Power-On Sequence Timing Diagram Rev.0.1

For Detail power sequence timing spec,  
please refer to #543016 chapter 43



teknisi indonesia



Rev	Description
R1.0	2019/07/02 1. Add R2324 for PCN sink current limit
	2019/07/05 1. Merge VCCPLL1/VCCPLL2 for power stage improve 2. R4305 change 8.25K for panel current limit 3. C0961_R6L and R7_0M change pin define
	2019/07/05 1. Reserve EC_USB test point for testing UMI2
	2019/07/8 1. Add R3224,R3225 for virtual wires test reserved 2. T0901_P04 connect 100 ohm follow R02 suggest 3. R0104/Audio delay card connector EC_USB
	2019/07/19 1. GP GPIO modify for NVOC solution 2. R077 module change to RP ROM number
	2019/07/23 1. Remove IO USB-A,Smart Antenna follow R05 modify 2. Add +1.2V_0V map follow AC simulation
	2019/07/25 1. Use 4 pin speaker 2. Update xSP connector 3. Modify Amp
	2019/07/29 1. Power circuit use minimum solution 2. Update T025 to add discharge bleeder resistor 3. Swap Type-C for layout
	2019/07/30 1. IO connector use 40 pin 2. Minimum Glide side
	2019/07/31 1.08 Reset circuit use Sleep IC for R0 (new)
	2019/08/01 1.Type-A ESD change part number: USB2 07024-01041000 2.Reserve EC GPIOs for GD IM_FMS0708 test: USB3 07024-00041000
	2019/08/01 1.C0961_0079_F0961_R0961 connect to GPR_00/GPR_01
	2019/08/03 1.Add P_33 sequence test point 2.Remove P3501,P3503,P3504,05054 3.R0302 connect to GND
	2019/08/05 1.USB connector pin definition modify 2.Add Type-C USB2 R20 component 3.Add USB2 port#6 check for DM
	2019/08/06 1.R2004,C2003 modify for 12V current limitation 2.R0 Reset circuit modify 3.J3106 reverse
	2019/08/07 1.USB3 C01/C02 Swap for layout 2.Replace R17 modify
	2019/08/12 1.VCC_AUDIO/1.1V/0.4V map modify follow AC simulation
	2019/08/13 1. 40M R400 use Codec part#? (Realtek suggest a follow R0443)
	2019/08/14 1. Add I2S anti-leakage circuit follow design IP 2.R2005 change U205
	2019/08/15 1. Add RS view hole and pad 2. GP ROM use UMI0 wire
	2019/08/21 1. Specr. change (1)Remove Proximity,0-Wensor,Audio Jack (2)Add DM0 (3)Type-A USB move to IO Board (4)QMC change to ZMC solution 2.Add +12V0_Gate Discharge 3.Uncount C2003,PCW026,09R024
	2019/08/22 1. Modify HDMI topology
	2019/08/26 1. Speaker wires connect to coded pin#1 2. Change U2012 footprint & symbol
	2019/08/29 1. PM_W080708 use AC GPIO UC pin high 10kohm
	2019/09/09 1. HDMI Receiver differential R20 component use 07024-01000000 2. HDMI I2C/AFIO R20 component use 07024-01020000
	2019/09/11 1. HDMI connect to CPU Display port F 2. HDMI R20 swap 3. IO connector pin swap 4. Remove I2S anti-leakage circuit (no ABC function)
	2019/09/12 1. add chock change to 0R022-01100010 2. Audio Panel_I07/P07A connect to GPR_015/D16 3. Add Type-C demp circuit 4. P-02 view hole modify
	2019/09/16 1. Mount R2011 follow ICL P05 2. Swap R0003/C0003 3. C1400,C1470,C1471 transference from 1.0V to 1.1V 4. Add C1474,C1475,C1476,C1659,C1660,C1661,C1662 (Follow simulation)
	2019/09/17 1. HDMI DM solution reduce side for layout 2. C1400 use QFN package 3. Swap C081 4. RS Show hole change

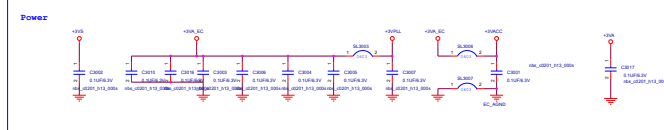
Customer Name

Only 3V Tolerance  
 GPB[0,1,2,3,4,5,6]  
 GPB[3,4,5,6,7]  
 GPB[0,4,6,7]  
 GPF[4,7]  
 GPF[6,7]  
 GPB[10,7]  
 GPB[10,7]

Can be adjusted to  
 Open-Drain for port:

GPB0-GPB3  
 GPB6-GPB7  
 GPF0-GPF7  
 GPB6-GPB7  
 GPF0-GPF7  
 GPB6-GPB6  
 GPB0-GPB5

EC ReguLow



GPB0-GPB3  
 GPB6-GPB7  
 GPF0-GPF7  
 GPB6-GPB7  
 GPF0-GPF7  
 GPB6-GPB6  
 GPB0-GPB5

EC ReguLow

GPB0-GPB3  
 GPB6-GPB7  
 GPF0-GPF7  
 GPB6-GPB7  
 GPF0-GPF7  
 GPB6-GPB6  
 GPB0-GPB5

GPB0-GPB3  
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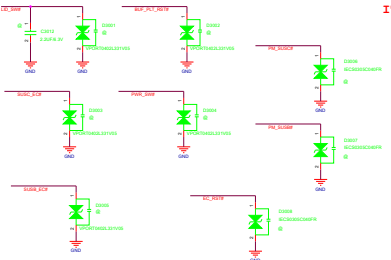
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 GPB6-GPB6  
 GPB0-GPB5

GPB0-GPB3  
 GPB6-GPB7  
 GPF0-GPF7  
 GPB6-GPB7  
 GPF0-GPF7  
 GPB6-GPB6  
 GPB0-GPB5

GPB0-GPB3  
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 GPB0-GPB5

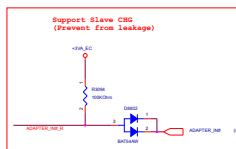
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EMI request

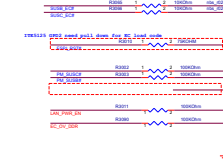


IT5125VG-128/CX (128KB) (06037-00370000) ?  
 IT5125VG-192/CX (192KB) (06037-00370200)

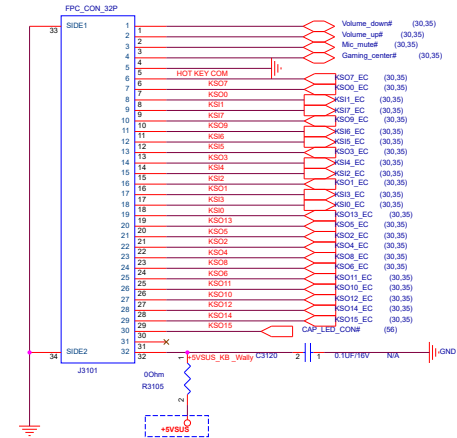
BGA 7.1\*7.1\*0.97



PM\_RDMUTE remove pull down @ EC side



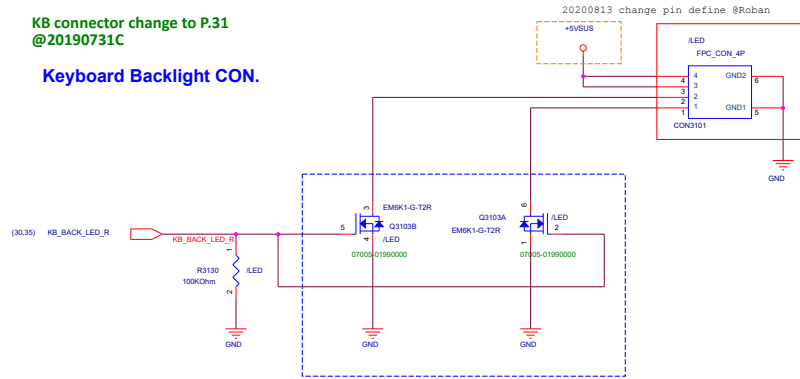
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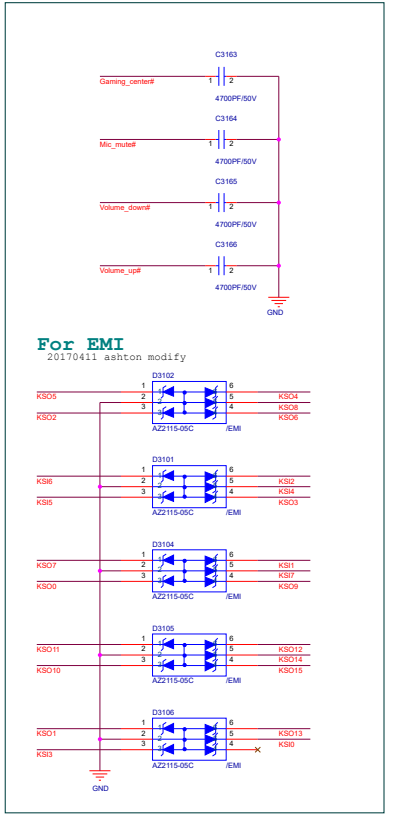
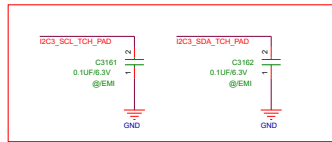
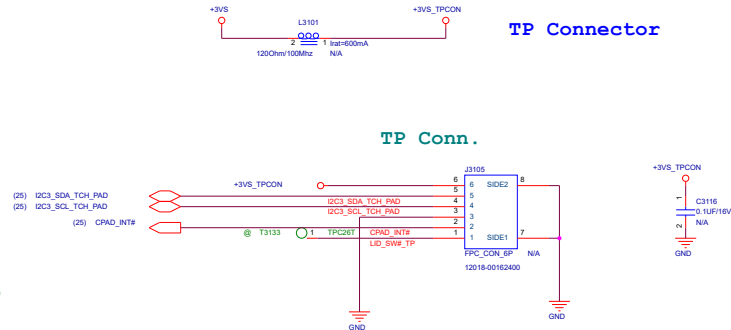
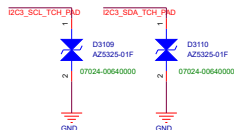
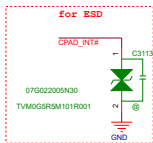
PIN_1	LED VCC
PIN_2	NC
PIN_3	CapsLock LED
PIN_4	K5015
PIN_5	K5014
PIN_6	K5012
PIN_7	K5010
PIN_8	K5011
PIN_9	K506
PIN_10	K508
PIN_11	K504
PIN_12	K502
PIN_13	K503
PIN_14	K54
PIN_15	K52
PIN_16	K501
PIN_17	K51
PIN_18	K5013
PIN_19	K506
PIN_20	K502
PIN_21	K504
PIN_22	K506
PIN_23	K5011
PIN_24	K501
PIN_25	K511
PIN_26	K500
PIN_27	K507
PIN_28	Hot key com
PIN_29	C4
PIN_30	C3
PIN_31	C2
PIN_32	C1

KB connector change to P.31  
@20190731C

Keyboard Backlight CON.



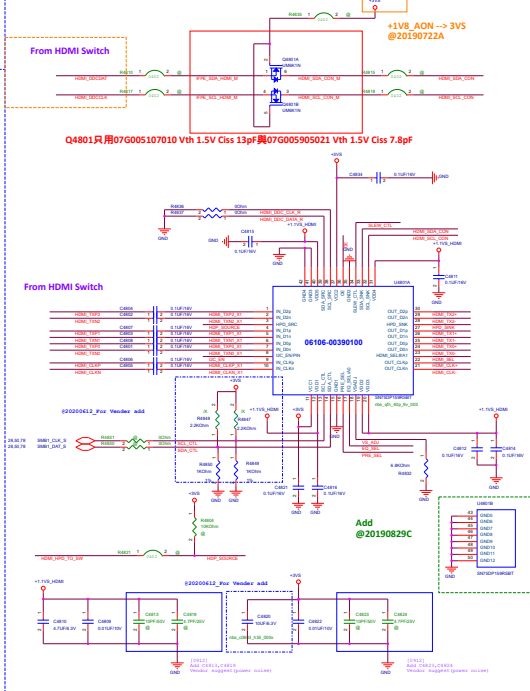
@20200619\_KB 耗電量320mA 換一顆MOS 400mA

For EMI  
20170411 ashton modifyEMI Reserve  
如要上件請確認容值(選擇Pico等級)D3110 ESD Diode  
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G  
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

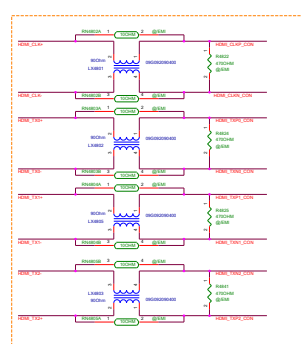
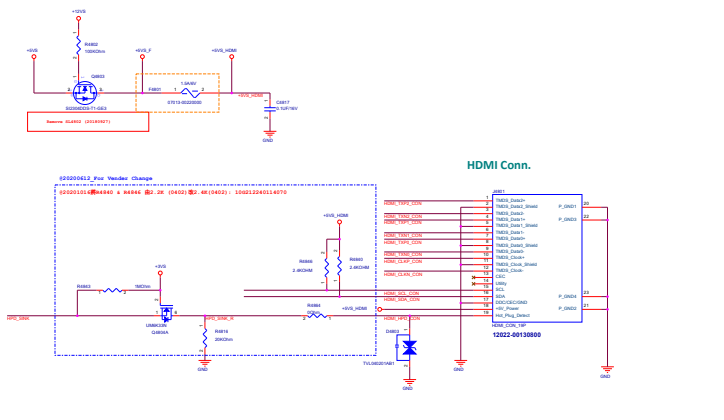
TP Conn.

&lt;Variant Name&gt;

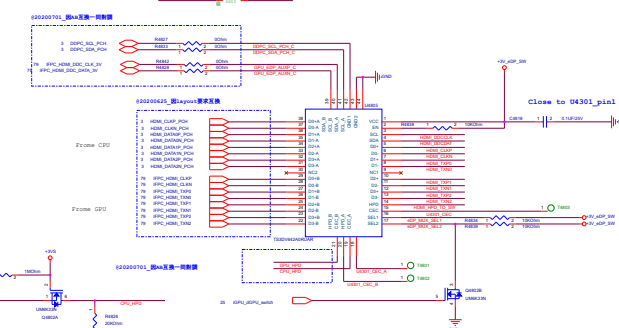
## Main Board

[illegible]

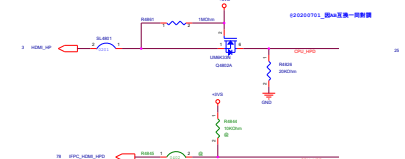
7



Add Co-lay device  
@20190626E

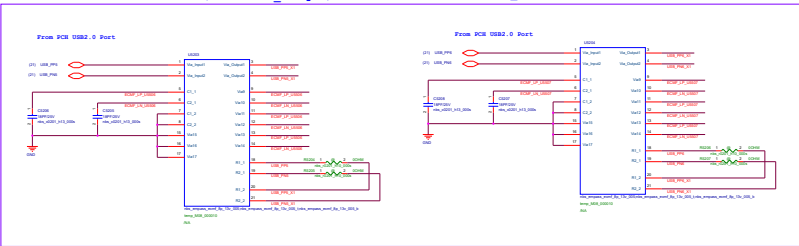


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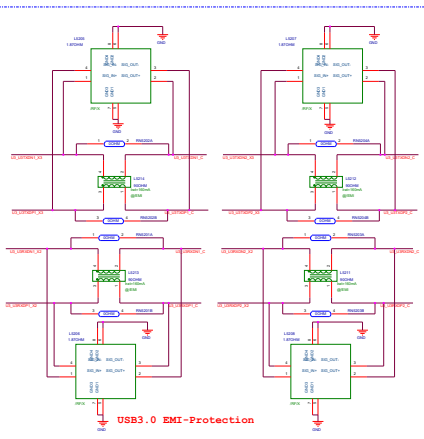
SR	SEL1	SEL2	FUNCTION
1	X	X	Switch Disabled, All Channel Hi-Z.
X	X	1	Channel 1 Enabled, Channel 3 Hi-Z. (Default)
X	X	X	Channel 1 Hi-Z, Channel 3 Enabled.

$\Delta CPO_{it} - \Delta CPO_{it-1}$ <i>waitcode</i>	$\Delta CPO_{it}$ 0	$\Delta CPO_{it}$ 1 (De Facto In)
---	------------------------	---

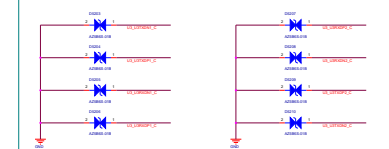


- Note : 1. This part & symbol only apply for standard PCB stack-up listed in datasheet appendix I  
Please check your project must matching the thickness , DF and DK value of PCB every layer  
2. C5504&C5503 / C5505&C5506 must be replaced with 10pF 0201 capacitors and the tolerance of capacitance value is 5%  
3. Pin7 & Pin8 & Pin11 & Pin12 must be connected to system ground  
4. Pin13 to Pin16 are floated in regular scheme

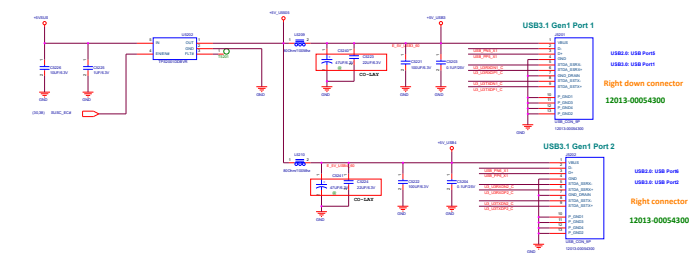
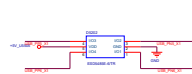
820200601 2P 20200612 1205-08  
820200601 2P 20200612 1205-08  
820200615 1201-14 20200612 1205-08



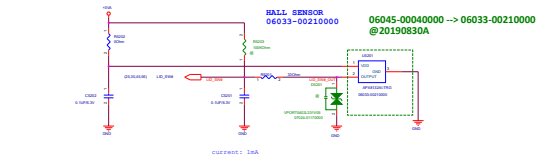
### USB3.0 ESD-Protection

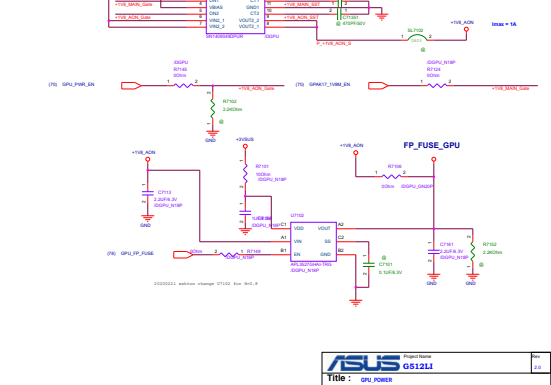
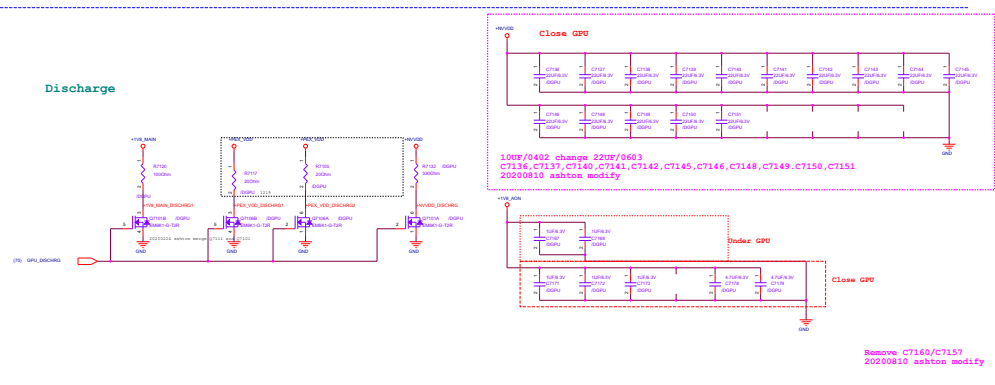
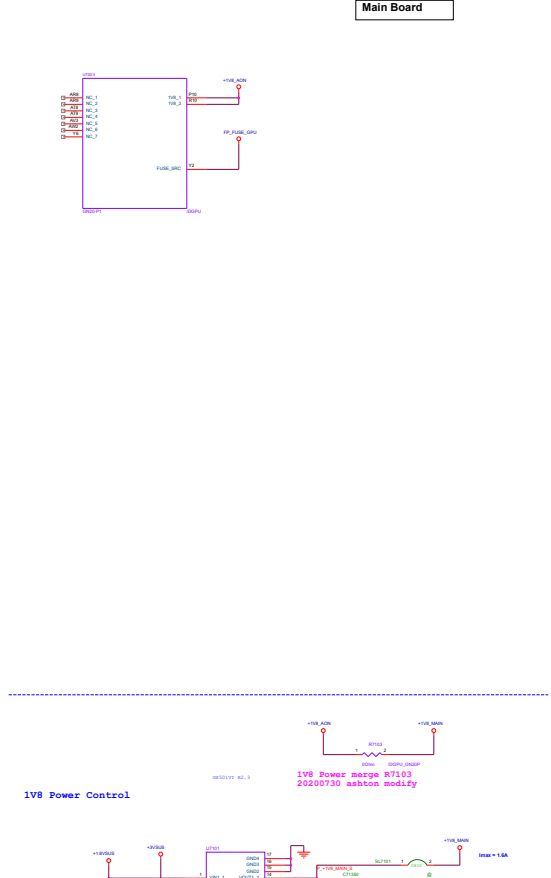
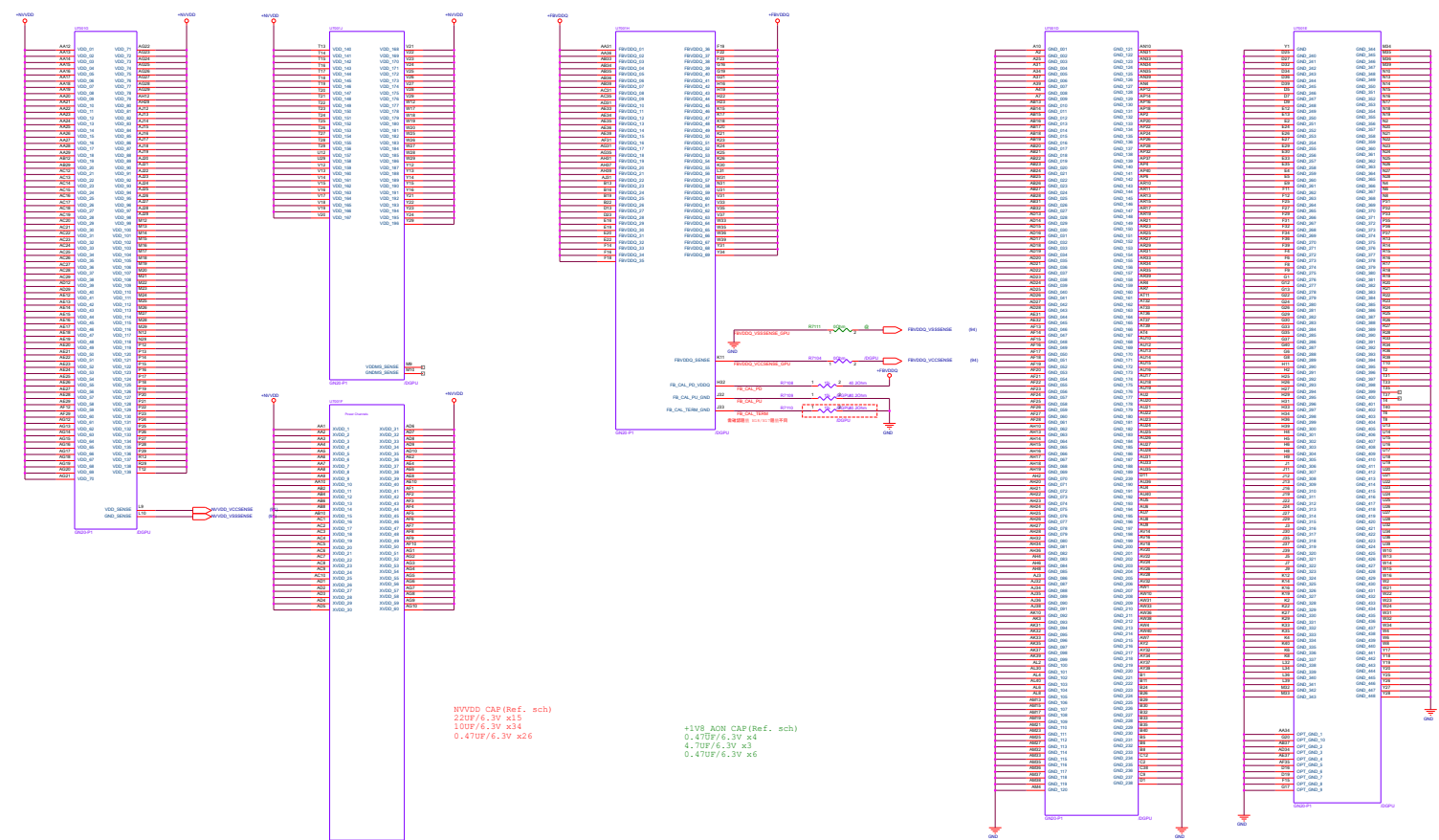


### USB2.0 ESD-Protection



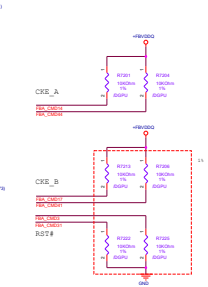
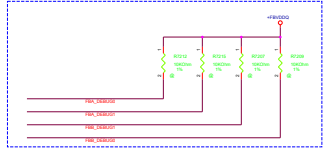
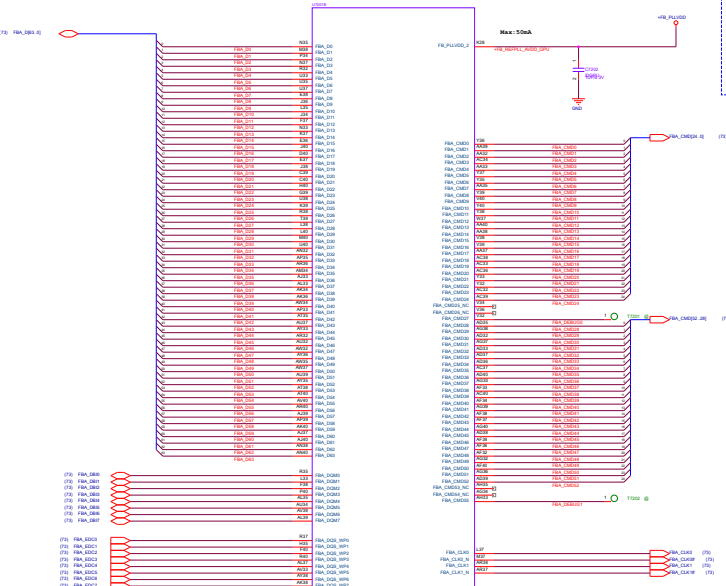
USB3.0\_Port1 & USB3.0\_Port2



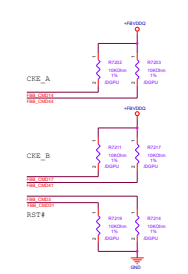
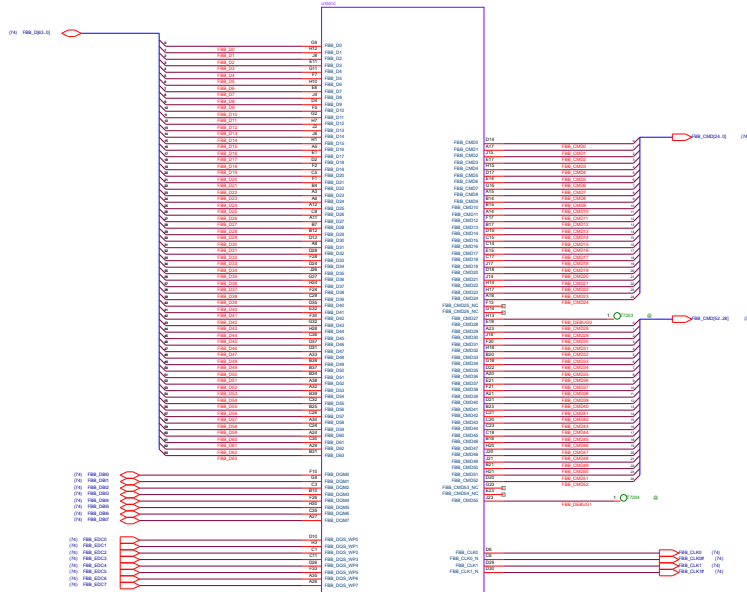




MEMORY: GPU FB Partition A



MEMORY: GPU FB Partition B



FB VREF N7205 and C7203  
035-128 pull down to 49.9 ohm +3.9 pF  
0858-128 Pull down to 2.49k ohm +3.9 pF  
20200730 ashton modify

Table 13 035-128 and 0858-128 FB BOM Differences		
FB Pin	What to do for 035-128	What to do for 0858-128
FB_VREF	Pull down to 49.9 ohm +3.9 pF Refer to N7205-607.4 for more details Platform Development Package (PDP-01900-001)	Pull down to 2.49 kΩ +3.9 pF

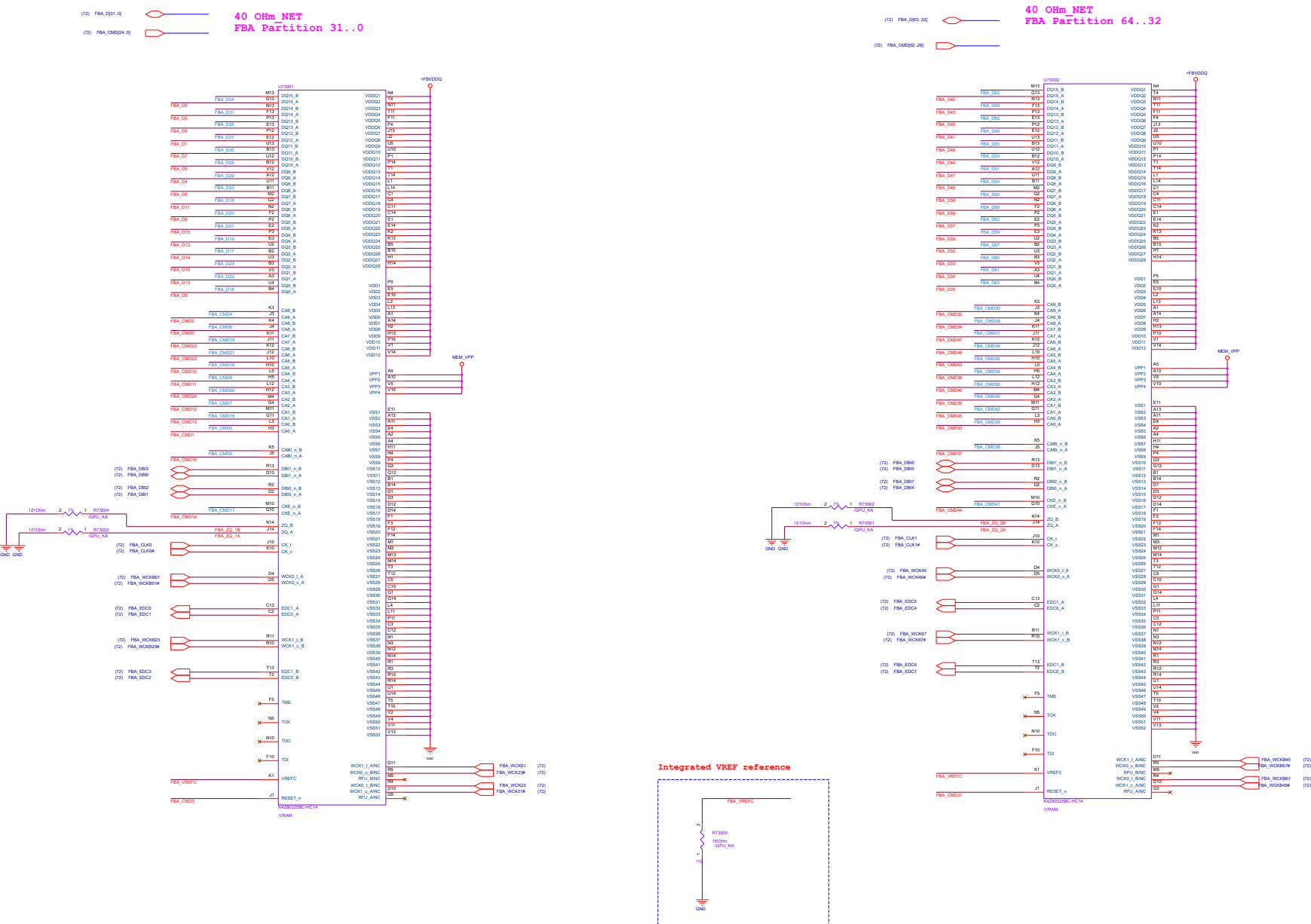
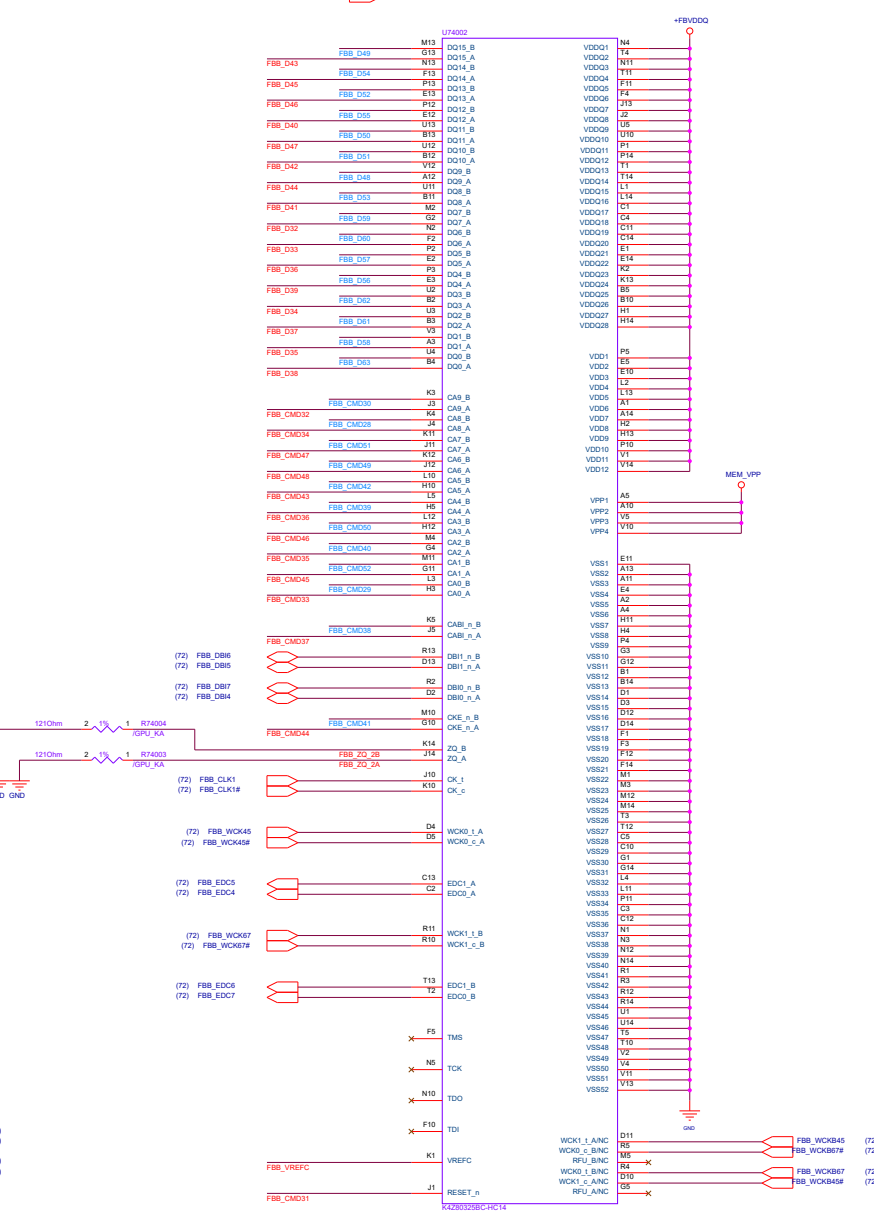
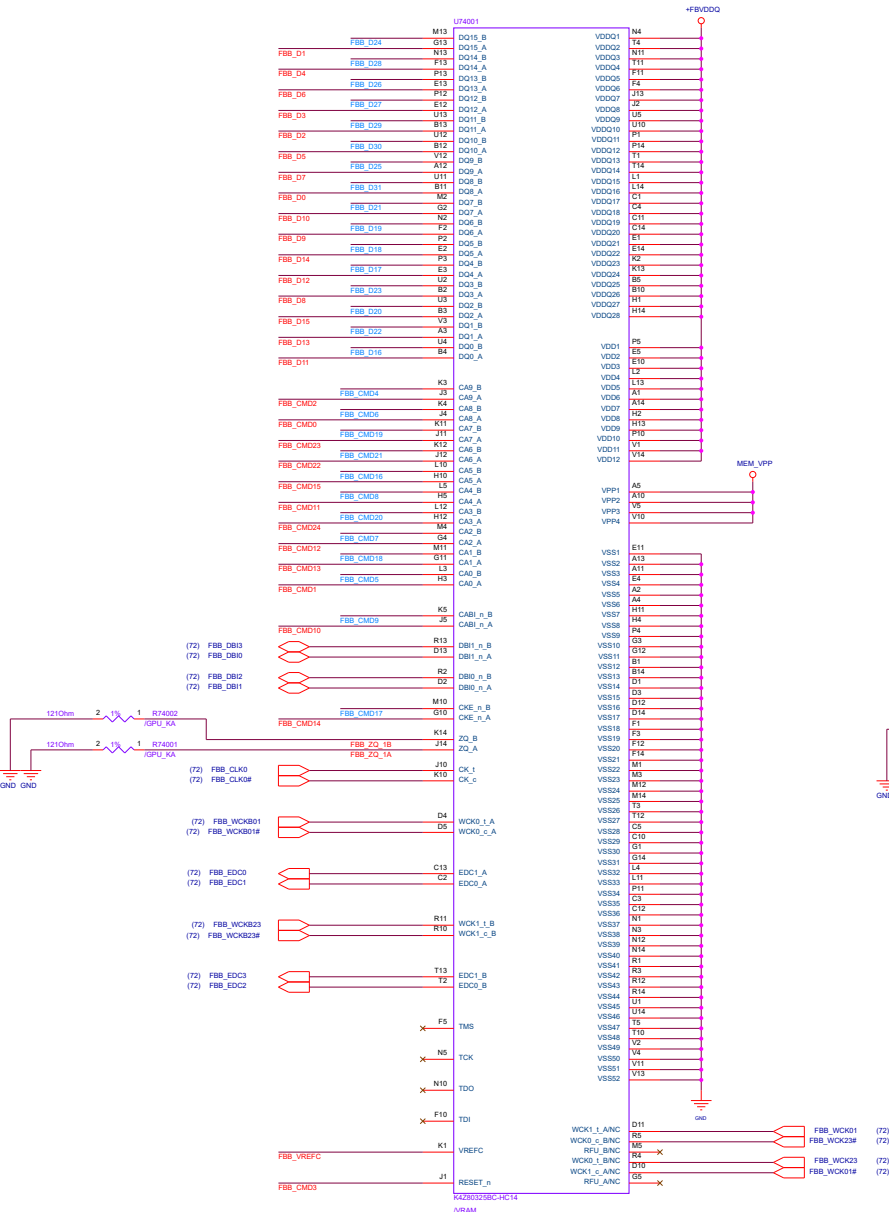


Table 4. N18P-G62/G61 GDDR6 Recommended Memories

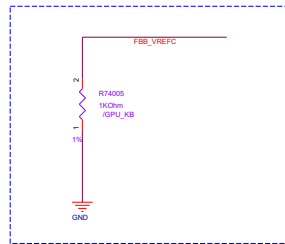
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.2V	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	Yes, TBD <sup>1</sup>	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	Yes, TBD <sup>2</sup>	Full	Production candidate

## Notes:

- For N18P-G62/G61, the maximum allowable memory case temperature is 95 °C.
- Requires Production GDDR6 with a specific date code restriction. Exact date code is currently TBD.



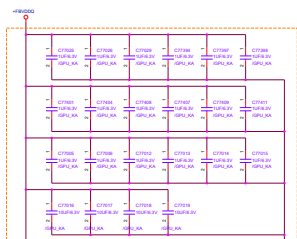
Integrated VREF reference



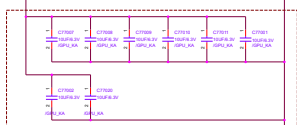
<Variant Name>

File	<Title>
Size	Document Number
C	G512L1
Date	Tuesday, December 20, 2020
Sheet	14 of 102
Rev	R1.0

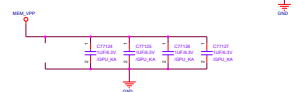
Under DRAM  
1uF x 18pcs  
10uF x 4pcs



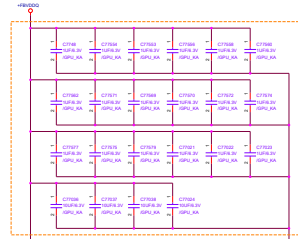
Around DRAM  
22uF x 6pcs  
10uF x 2pcs



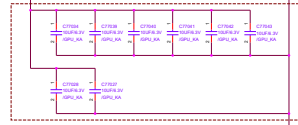
Under DRAM  
1uF x 4pcs  
4.7uF x 1pcs



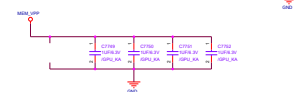
Under DRAM  
1uF x 18pcs  
10uF x 4pcs



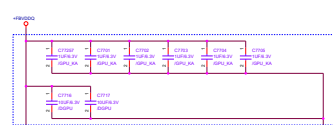
Around DRAM  
22uF x 6pcs  
10uF x 2pcs



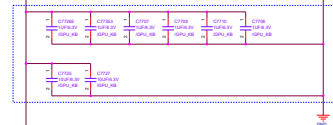
Under DRAM  
1uF x 4pcs  
4.7uF x 1pcs



Partition A  
Under GPU  
1uF x 6pcs  
10uF x 2pcs



Partition B  
Under GPU  
1uF x 6pcs  
10uF x 2pcs



Close GPU  
10uF x 2pcs  
22uF x 5pcs

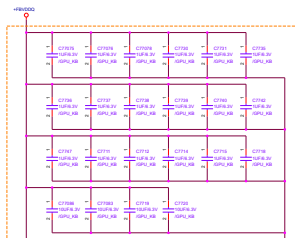


FBVDDQ (GPU side) <sup>1</sup>	1.35V 1.5V	24 x 0.47uF (0201W X65) 4 x 10uF (0603 X65)	2 x 10uF (0603 X65) <sup>2</sup> 5 x 22uF (0603 X65)
Alternate solution: 12 x 1uF (0402 or 0201W, X65) <sup>3</sup> 4 x 10uF (0603 X65)			

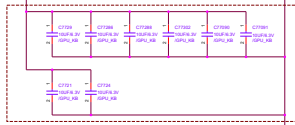
Table 8.12 DRAM-Side Decoupling

Decoupling Capacitors		Recommended Quantity and Placement (per DRAM device)	
Capacitance	Type, [Size <sup>NOTE 1</sup> ]	Quantity	Placement
VDD/VDDQ Rail			
0.47 uF <sup>NOTE 2</sup>	X65 [0201W]	36	Under or very close to DRAM
10 uF	X65 [0603]	4	
10 uF	X65 [0603]	2	
22 uF	X65 [0603]	6	Around DRAM
VPP Rail			
0.47 uF <sup>NOTE 3</sup>	X65 [0201W]	4	Under or very close to DRAM
4.7 uF	X65 [0603]	1	

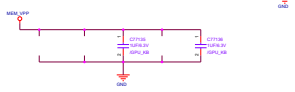
Under DRAM  
1uF x 18pcs  
10uF x 4pcs



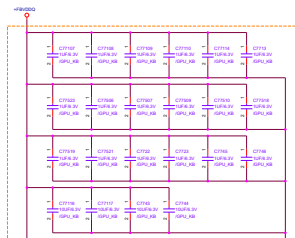
Around DRAM  
22uF x 6pcs  
10uF x 2pcs



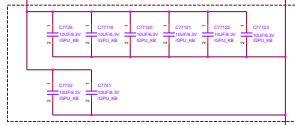
Under DRAM  
1uF x 4pcs  
4.7uF x 1pcs



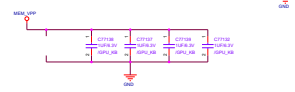
Under DRAM  
1uF x 18pcs  
10uF x 4pcs



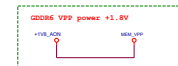
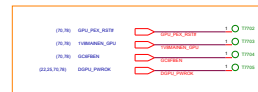
Around DRAM  
22uF x 6pcs  
10uF x 2pcs



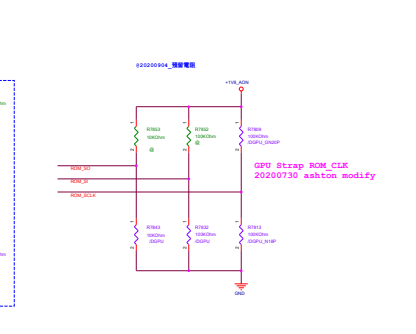
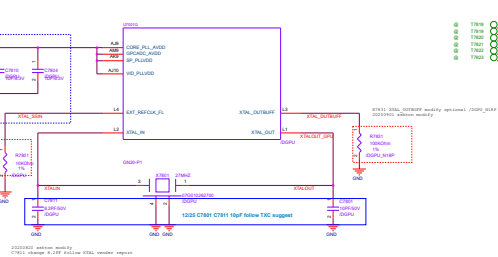
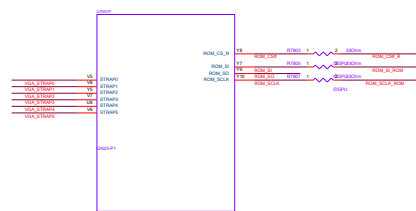
Under DRAM  
1uF x 4pcs  
4.7uF x 1pcs



For power sequence measurement

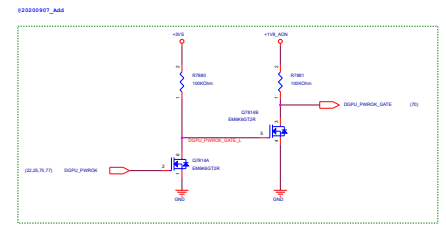
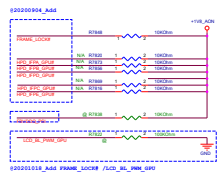
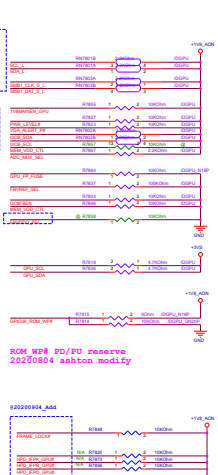


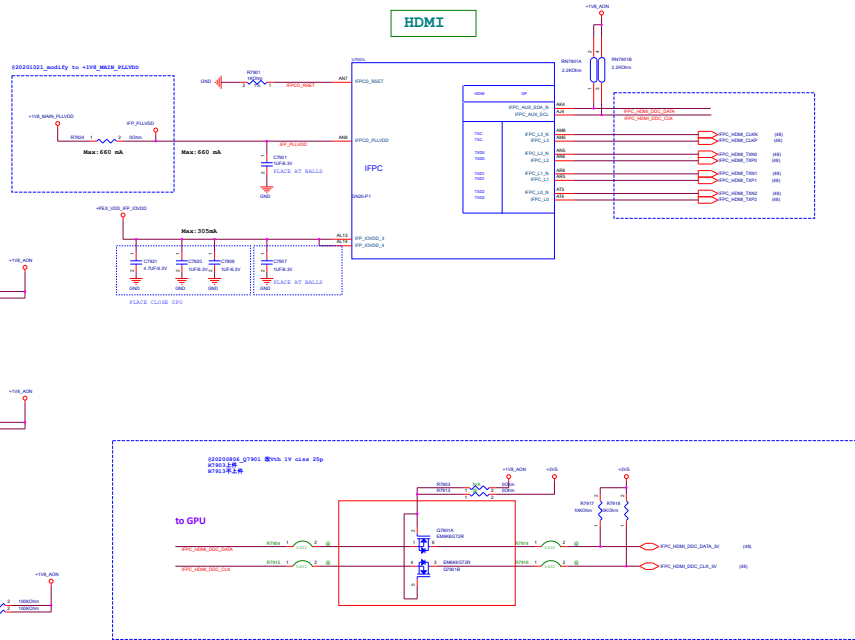
0201W 0.47uF (0201W, X65) 1.35V 1.5V



	GB5B-128
K) to (L,	<p>Set (ROM_SO, ROM_SI, ROM_CLK) to (L, L, H) to enable FS_OVERT</p> <ul style="list-style-type: none"> <li>• ROM_SI and ROM_CLK: 100 kΩ</li> <li>• ROM_SO: 10 kΩ</li> </ul>
	<ul style="list-style-type: none"> <li>• SMB_ALT_ADDR</li> <li>• DEVID_SEL</li> <li>• PCIE_CFG</li> <li>• VGA_DEVICE</li> </ul> <p>RAMCFG[4:0]</p>

	GB5B-128
K) to (L,	<p>Set (ROM_SO, ROM_SI, ROM_CLK) to (L, L, H) to enable FS_OVERT</p> <ul style="list-style-type: none"> <li>• ROM_SI and ROM_CLK: 100 kΩ</li> <li>• ROM_SO: 10 kΩ</li> </ul>
	<ul style="list-style-type: none"> <li>• SMB_ALT_ADDR</li> <li>• DEVID_SEL</li> <li>• PCIE_CFG</li> <li>• VGA_DEVICE</li> </ul> <p>RAMCFG[4:0]</p>





## +3VA\_DSW / +5VSUS [System Power]



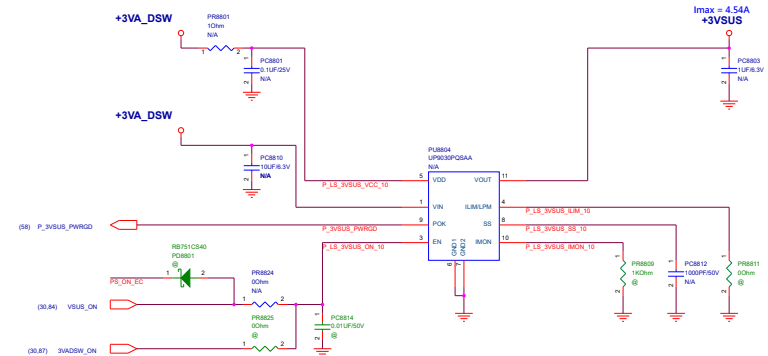
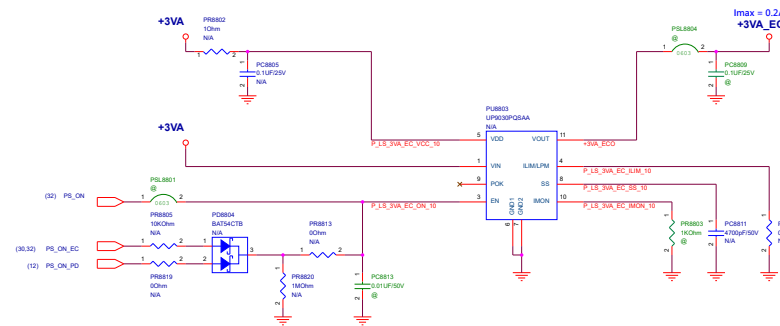
### Adaptor Mode (IMVP8)

### Battery Mode (IMVP8)

PT870\* 請放置 PU8700旁;並請放置Trace 上!

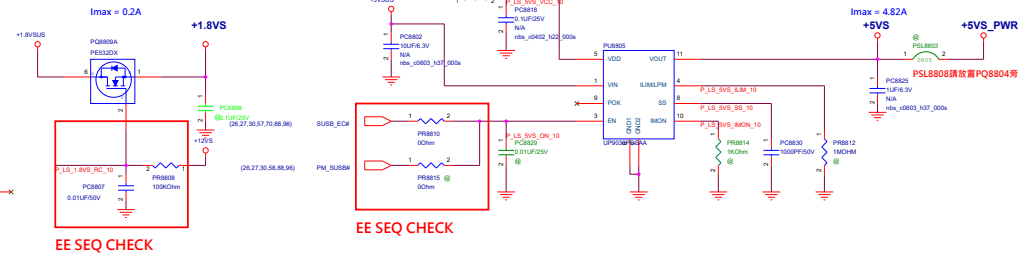
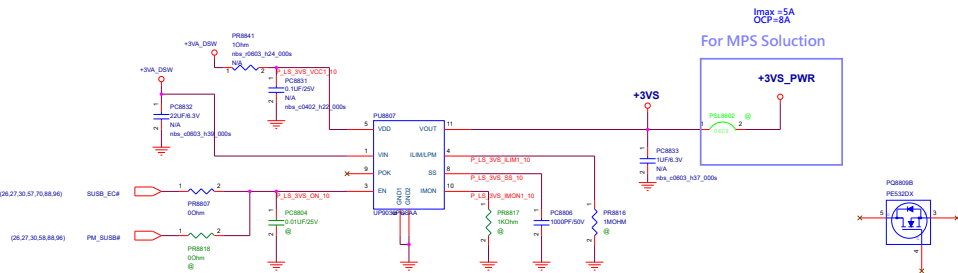


## Load Switch



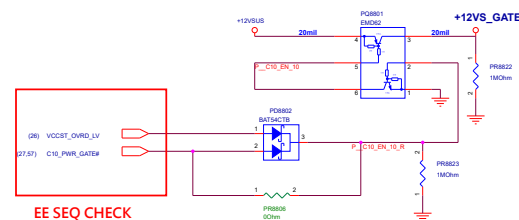
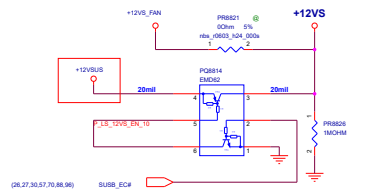
### uP9030 ILIM/LPM Setting 對應表

ILIM PIN	LPM (C10)	LIMIT Current
GND	Off	3A
1M to GND	Off	5A
Float/VDD	On	8A



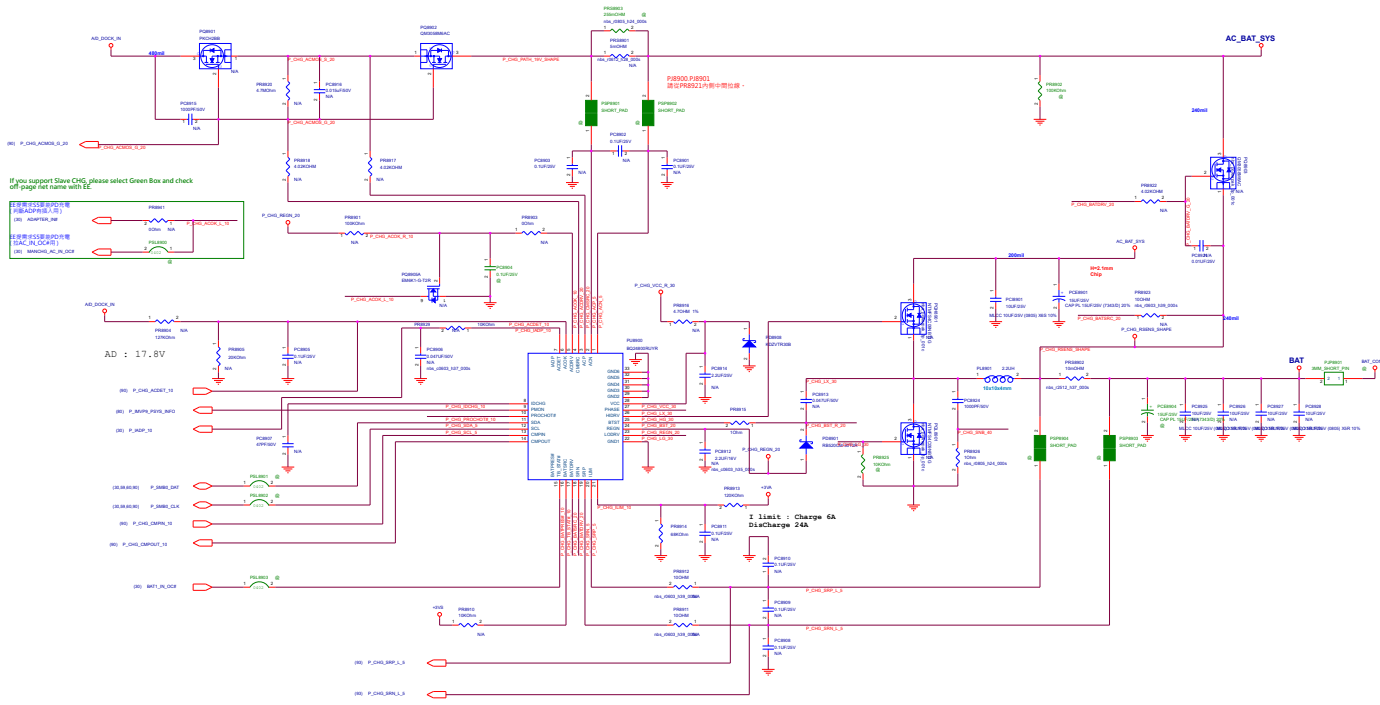
### +12VS 的 Vin 對應 BOM 表

	+12V5_FAN	+12V5U5
PR8821	N/A	⊗
PR8826	⊗	N/A
PQ8814	⊗	N/A



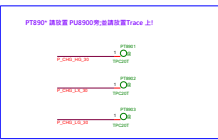


PSB901	ADP<120W	ADP<200W	ADP<200W	ADP<330W
	TBD	5m	5m	2m
	TBD	1212L-00080001	1212L-00080001	1212L-00080001



If you support SWS please select Green Box and check off page (set name with LE)

ADAPTER\_PWR  
TACN\_PN\_204511  
MAXIMUM\_PWR\_204511



Adaptor select  
total power = 90% ADP

The diagram illustrates a power distribution circuit. On the left, a power source labeled 'PSB901' is connected to a switch labeled 'SW1'. The switch is connected to a relay labeled 'RELAY'. The relay is connected to a load labeled 'PSB936'. The load is connected to ground. The diagram also shows the connection between the power source and the load through the switch and relay. The power source is connected to the switch, which is connected to the relay, which is connected to the load. The load is connected to ground. The diagram also shows the connection between the power source and the load through the switch and relay.

Adaptor select			
		10m	5m
PSB901		10m	5m
PSB936		10m	5m
120	0.4V	45W	120W
120	0.8V	150W	150W
120	1.2V	180W	180W
120	1.6V	65W	230W
120	2.0V	NA	280W
120	2.4V	90W	200W
120	2.8V	120W	240W

